DAFTAR LAMPIRAN

Lampiran 1 Datasheet IC NE 555 Dan SCE FIR 3D

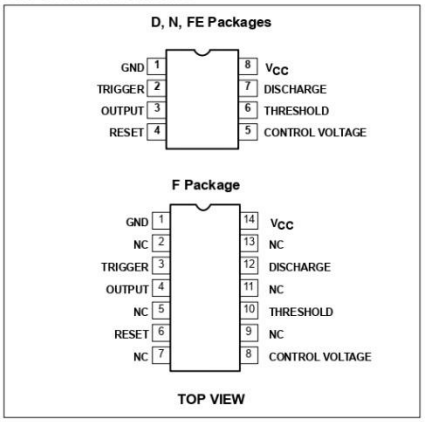
- IC NE 555

Timer | **NE/SA/SE555/SE555C**

DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

PIN CONFIGURATIONS



FEATURES

- Turn-off time less than 2μs
- Max. operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE555D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE555N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA555N	0404B
8-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA555D	0174C
8-Pin Hermetic Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CFE	
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555CN	0404B
14-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555N	0405B
8-Pin Hermetic Cerdip	-55°C to +125°C	SE555FE	
14-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CF	0581B

- SCR FIR 3D

DATA SHEET

NEC

THYRISTORS

03P4MG,03P6MG

300 mA HIGH-WITHSTANDING-VOLTAGE MOLD SCR

DESCRIPTION

The 03P4MG and 03P6MG are P-gate fully diffused mold SCRs with an average on-state current of 300 mA. The repeat peak off-state voltages (and reverse voltages) are 400 and 600 V.

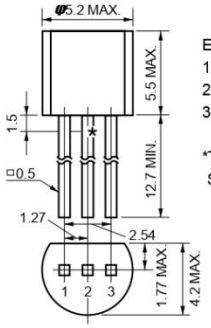
FEATURES

- 400 and 600 V high-withstanding-voltage series of products
- The non-repetitive withstanding voltage is a high 700 V, making it easy to harmonize the rise voltage of the surge absorber.
- High-sensitivity thyristor (I_{GT} = 3 to 50 μA)
- Employs flame-retardant epoxy resin (UL94V-0)

APPLICATIONS

Leakage breakers, SSRs, various type of alarms, consumer electronic equipments and automobile electronic components

PACKAGE DRAWING (Unit: mm)



Electrode connection
1: Gate
2: Anode
3: Cathode

*T_C test bench-mark
Standard weight: 0.3 g

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

	Parameter	Symbol	Ratings		Unit	Remarks
			03P4MG	03P6MG		
	Non-repetitive Peak Reverse Voltage	V_{RSM}	700	700	V	R_{GK} = 1 kΩ
	Non-repetitive Peak Off-state Voltage	V_{DSM}	700	700	V	R_{GK} = 1 kΩ
	Repetitive Peak Reverse Voltage	V_{RRM}	400	600	V	R_{GK} = 1 kΩ
	Repetitive Peak Off-state Voltage	V_{DRM}	400	600	V	R_{GK} = 1 kΩ
	Average On-state Current	$I_{T(AV)}$	300 (T_A = 30°C, Single half-wave, θ = 180°)		mA	Refer to Figure 10.
	Effective On-state Current	$I_{T(RMS)}$	470		mA	–
★	Surge On-state Current	I_{TSM}	8 (f = 50 Hz, Sine half-wave, 1 cycle)		A	Refer to Figure 2.
	Fusing Current	$\int i^2dt$	0.15 (1 ms ≤ t ≤ 10 ms)		A^2s	–
	Critical Rate of On-state Current of Rise	dI_T/dt	20		A/μs	–
	Peak Gate Power Dissipation	P_{GM}	100 (f ≥ 50 Hz, Duty ≤ 10%)		mW	Refer to Figure 3.
	Average Gate Power Dissipation	$P_{G(AV)}$	10		mW	Refer to Figure 3.
	Peak Gate Forward Current	I_{FGM}	100 (f ≥ 50 Hz, Duty ≤ 10%)		mA	–
	Peak Gate Reverse Voltage	V_{RGM}	6		V	–
	Junction Temperature	T_j	−40 to +125		°C	–
	Storage Temperature	T_{stg}	−55 to +150		°C	–

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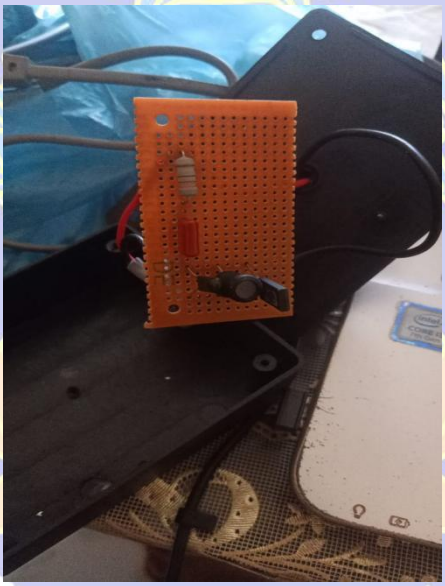
The mark ★ shows major revised points.

Lampiran 2 Dokumentasi Pembuatan Alat

(TRANSMITER)



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Lampiran 3 Dokumentasi Pengujian Alat