DAFTAR LAMPIRAN

Lampiran 1 Data Sheet Mosfet IRFZ44N dan IC TL494

- Mosfet IRFZ44N

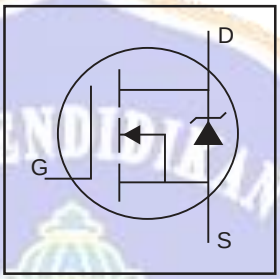
International
IOR Rectifier

PD - 94787B

IRFZ44NPbF

HEXFET® Power MOSFET

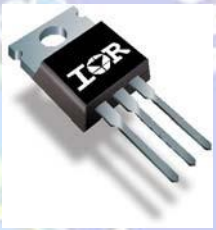
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast *Switching*
- Fully Avalanche Rated
- Lead-Free



V_{DSS} = 55V

$R_{DS(on)}$ = 17.5mΩ

I_D = 49A



TO-220AB

Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to AChieve extremely low on-resistance per silicon area. This benefit, combined with the fast *switching* speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 pACkage is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low pACkage cost of the TO-220 contribute to its wide ACceptance throughout the industry.

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	49	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	35	
I_{DM}	Pulsed Drain Current	160	
P_D @T_C = 25°C	Power Dissipation	94	W
	Linear Derating FACtor	0.63	W/°C
V_{GS}	*Gate*-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current	25	A
E_{AR}	Repetitive Avalanche Energy	9.4	mJ
dv/dt	Peak Diode Recovery dv/dt	5.0	V/ns

T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.5	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased SurfACe	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

Electrical CharACteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.058	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	17.5	mΩ	V_{GS} = 10V, I_D = 25A
$V_{GS(th)}$	*Gate* Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	19	——	——	S	V_{DS} = 25V, I_D = 25A
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	µA	V_{DS} = 55V, V_{GS} = 0V
		——	——	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	*Gate*-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
Q_g	Total *Gate* Charge	——	——	63	nC	I_D = 25A V_{DS} = 44V V_{GS} = 10V, See Fig. 6 and 13
Q_{gs}	*Gate*-to-Source Charge	——	——	14		
Q_{gd}	*Gate*-to-Drain ("Miller") Charge	——	——	23		
$t_{d(on)}$	Turn-On Delay Time	——	12	——	ns	V_{DD} = 28V I_D = 25A R_G = 12Ω V_{GS} = 10V, See Fig. 10
t_r	Rise Time	——	60	——		
$t_{d(off)}$	Turn-Off Delay Time	——	44	——		
t_f	Fall Time	——	45	——		
L_D	Internal Drain Inductance	——		——	nH	Between lead, 6mm (0.25in.) from pACkage and center of die contACt
L_S	Internal Source Inductance	——		——		
C_{iss}	Input CapACitance	——	1470	——	pF	V_{GS} = 0V V_{DS} = 25V *f* = 1.0MHz, See Fig. 5
C_{oss}	Output CapACitance	——	360	——		
C_{rss}	Reverse Transfer CapACitance	——	88	——		
E_{AS}	Single Pulse Avalanche Energy	——	530	150	mJ	I_{AS} = 25A, L = 0.47mH

Source-Drain Ratings and CharACteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	49		MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)	——	——	160		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 25A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	——	63	95	ns	T_J = 25°C, I_F = 25A di/dt = 100A/µs
Q_{rr}	Reverse Recovery Charge	——	170	260	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

- **Lampiran Data Sheet IC TL494**

Description

The TL494 device incorporates all the functions required in the construction of a pulse-widthmodulation (PWM) control circuit on a single chip. Designed primarily for power-supply control, this device offers the flexibility to tailor the power-supply control circuitry to a specific application.

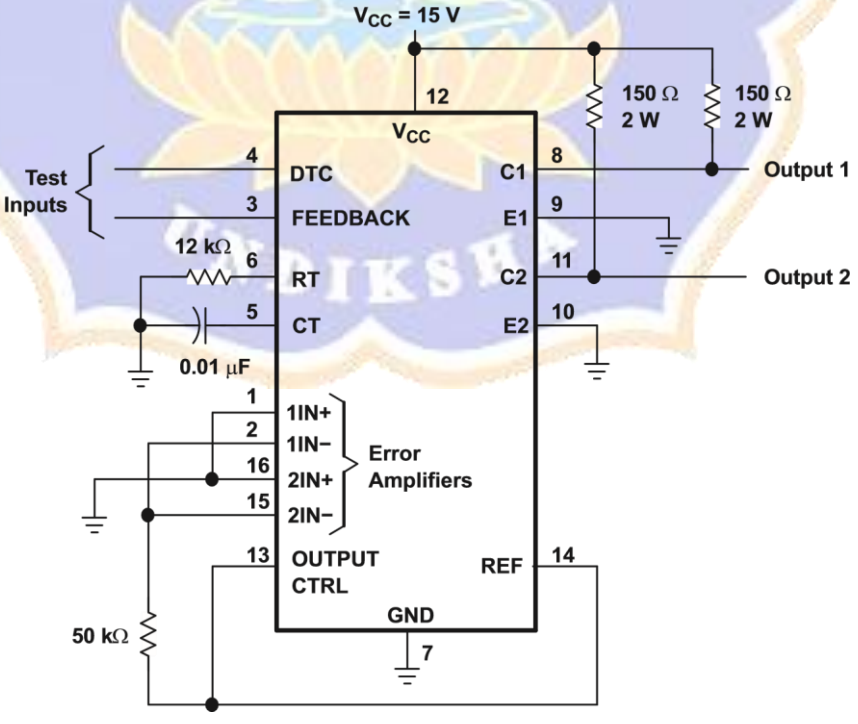
The TL494 device contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, a 5-V, 5%-precision regulator, and output-control circuits.

The error amplifiers exhibit a common-mode voltage range from –0.3 V to V_{CC} – 2 V. The dead-time control comparator has a fixed offset that provides approximately 5% dead time. The on-chip oscillator can be bypassed by terminating RT to the reference output and providing a sawtooth input to CT, or it can drive the common circuits in synchronous multiple-rail power supplies.

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. The TL494 device provides for push-pull or singleended output operation, which can be selected through the output-control function. The architecture of this device prohibits the possibility of either output being pulsed twice during push-pull operation.

The TL494 device is charACterized for operation from 0°C to 70°C. The TL494I device is charACterized for operation from –40°C to 85°C.

Parameter Measurement Information



TEST CIRCUIT

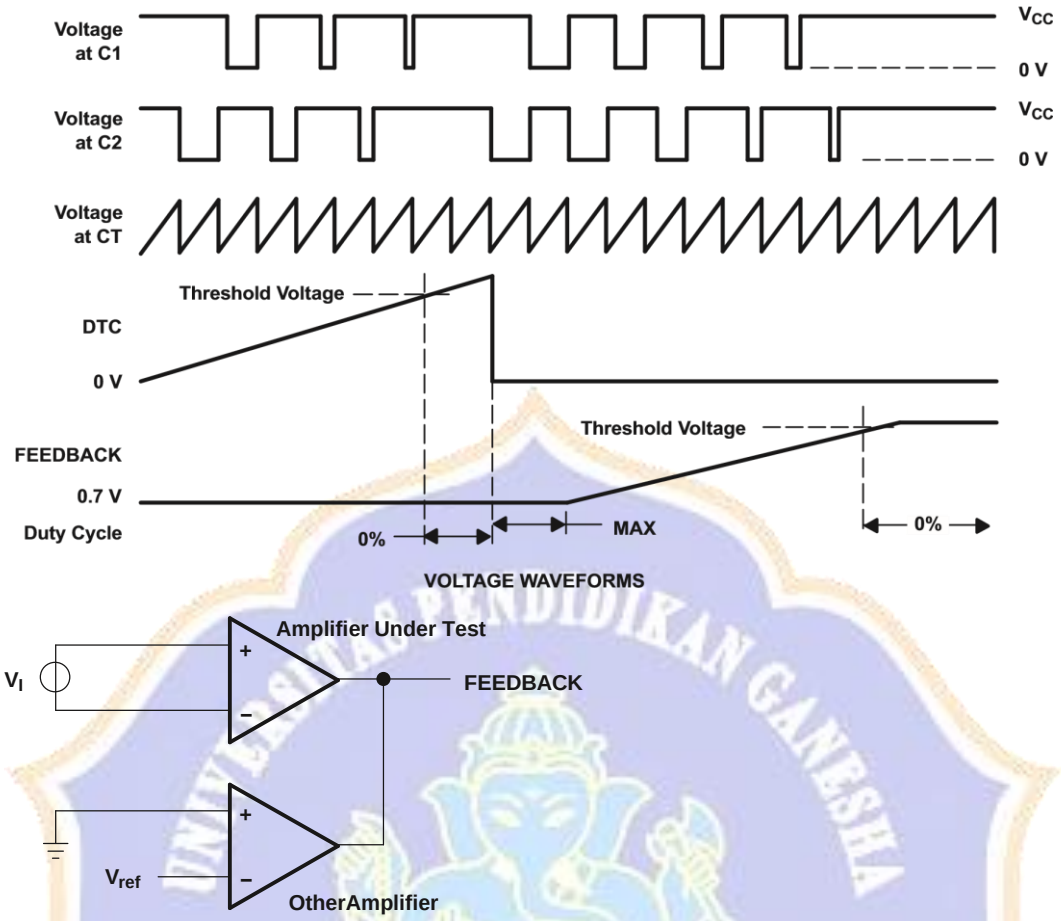
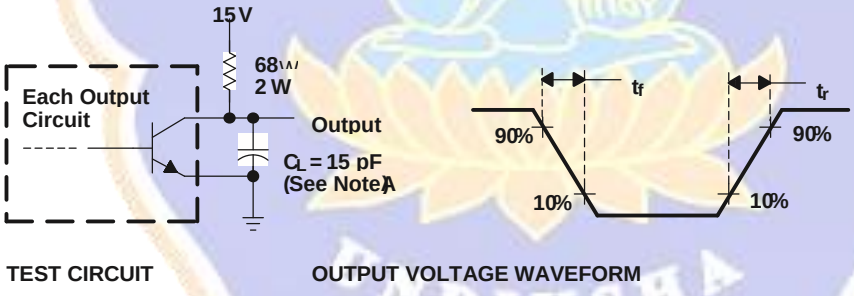
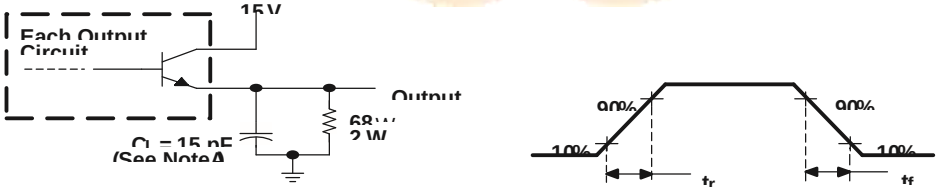


Figure 8-2. Amplifier CharACteristics



NOTE A: C_L includes probe and jig capACitance.

Figure 8-3. Common-Emitter Configuration



NOTE A: C_L includes probe and jig capACitance.

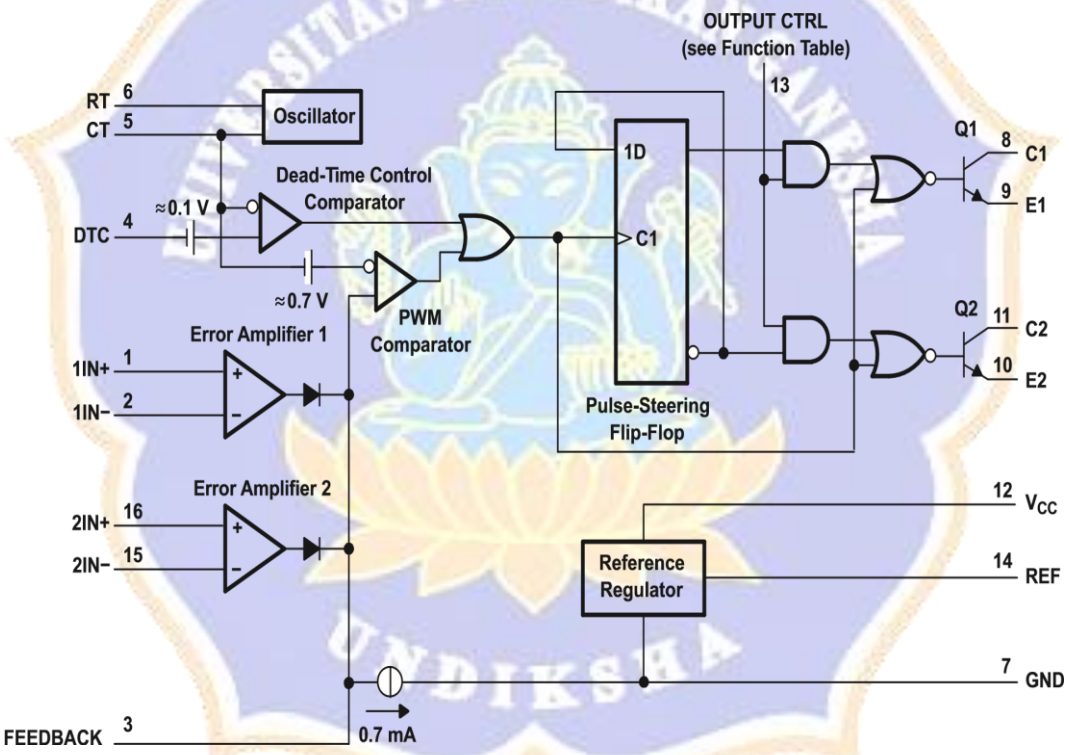
Figure 8-4. Emitter-Follower Configuration

9 Detailed Description

Overview

The design of the TL494 not only incorporates the primary building blocks required to control a *switching* power supply, but also addresses many basic problems and reduces the amount of additional circuitry required in the total design. The TL494 is a fixed-frequency pulse-width-modulation (PWM) control circuit. Modulation of output pulses is ACcomplished by comparing the sawtooth waveform created by the internal oscillator on the *timing* capACitor (CT) to either of two control signals. The output stage is enabled during the time when the sawtooth voltage is greater than the voltage control signals. As the control signal increases, the time during which the sawtooth input is greater decreases; therefore, the output pulse duration decreases. A pulse-steering flip-flop alternately directs the modulated pulse to eACh of the two output transistors. For more information on the operation of the TL494, see the application notes located on ti.com.

Functional Block Diagram



Feature Description

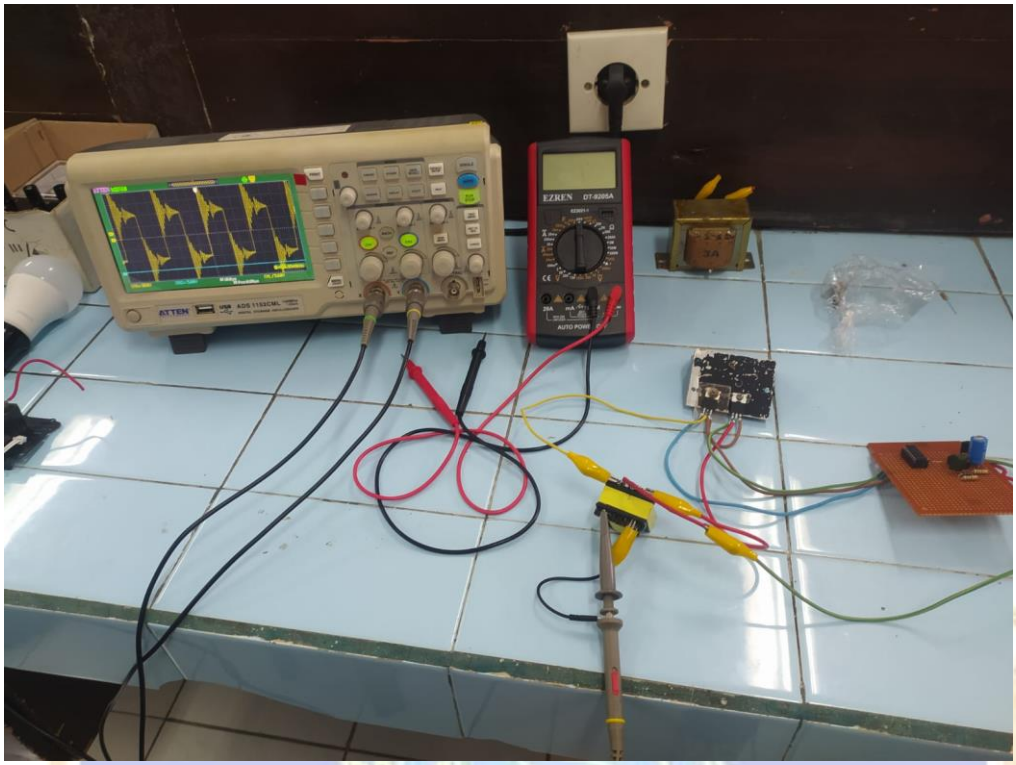
5-V Reference Regulator

The TL494 internal 5-V reference regulator output is the REF pin. In addition to providing a stable reference, it ACts as a preregulator and establishes a stable supply from which the output-control logic, pulse-steering flip-flop, oscillator, dead-time control comparator, and PWM comparator are powered. The regulator employs a band-gap circuit as its primary reference to maintain thermal stability of less than 100-mV variation over the operating free-air temperature range of 0°C to 70°C. Short-circuit protection is

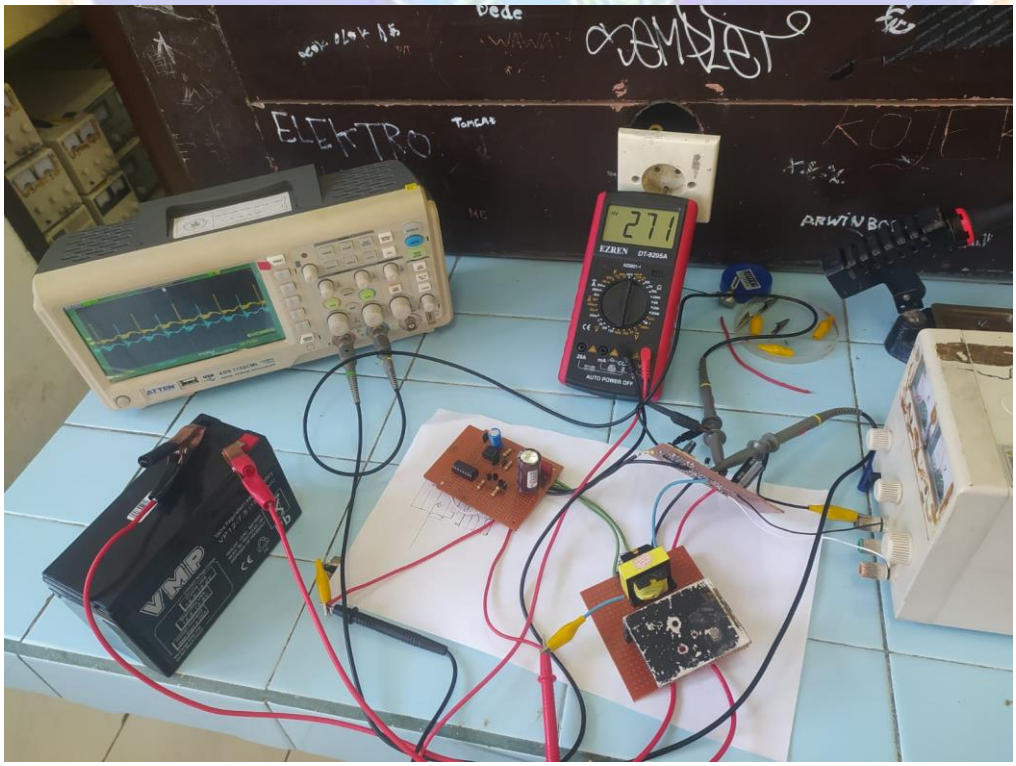
provided to protect the internal reference and preregulator; 10 mA of load current is available for additional bias circuits. The reference is internally programmed to an initial ACcurACy of ±5% and maintains a stability of less than 25-mV variation over an input voltage range of 7 V to 40 V. For input voltages less than 7 V, the regulator saturates within 1 V of the input and trACks it.

Lampiran Dokumentasi Perancangan dan Pengujian

1. Dokumentasi Perancangan gelombang keluaran dengan IC 4017 dan NE555

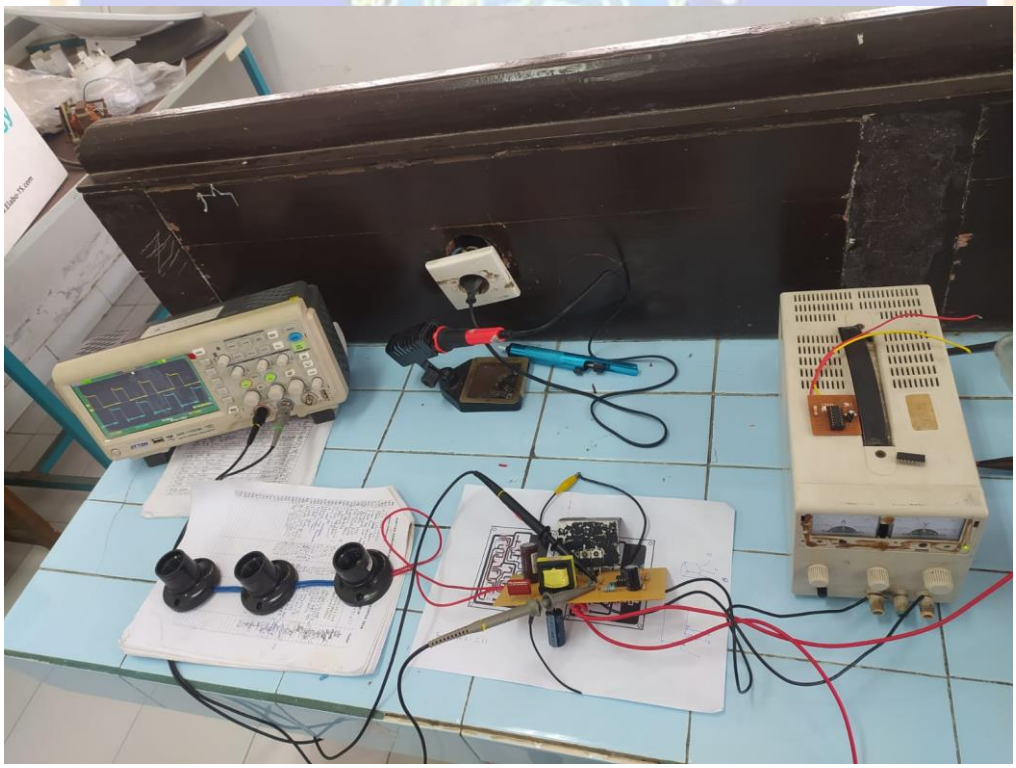


2. Dokumentasi pengujian tegangan keluaran dengan IC 4017 dan NE555

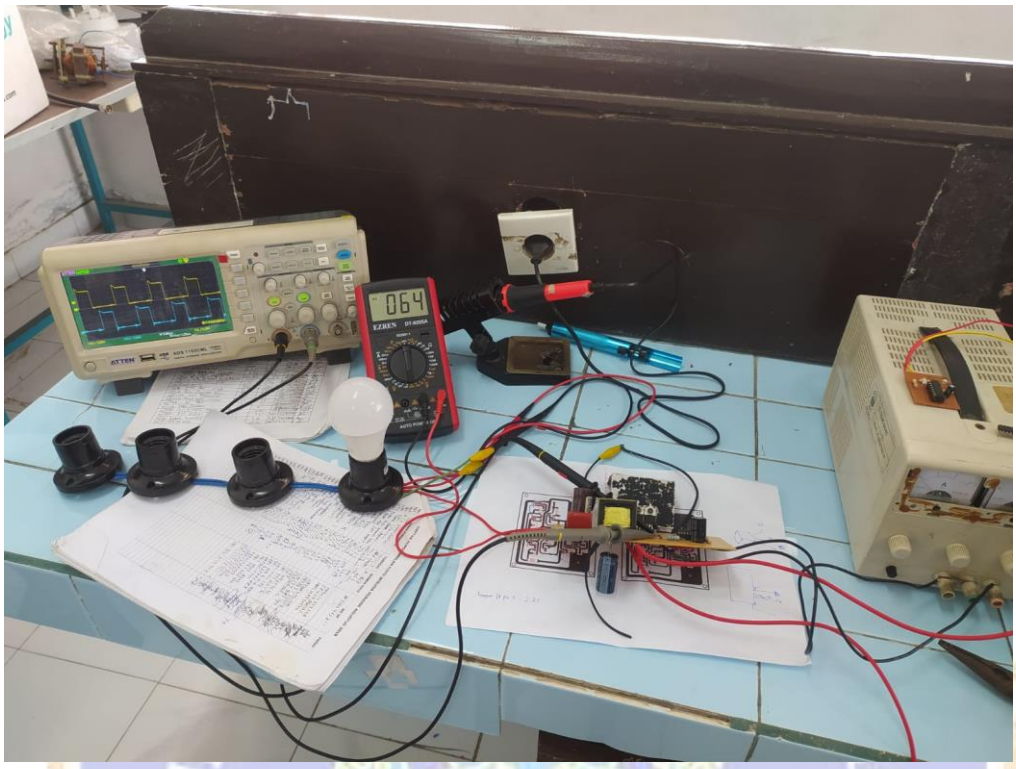


3. Dokumentasi pengujian tegangan output rangkaian inverter dan converter

4. Dokumentasi pengujian output converter tanpa beban

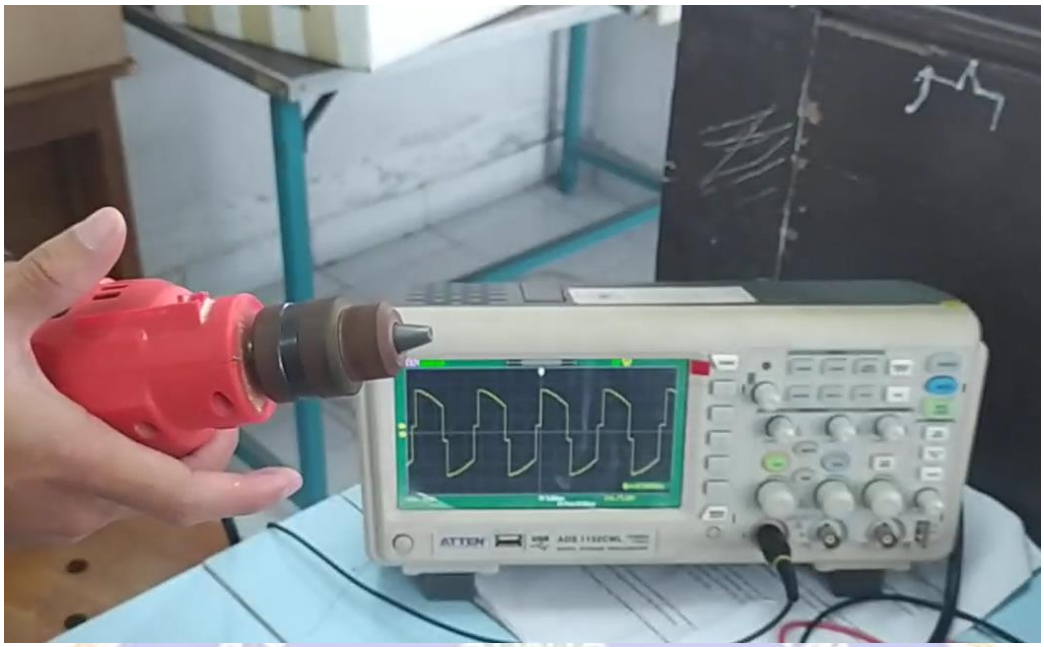


5. Dokumentasi pengujian converter dengan beban satu lampu



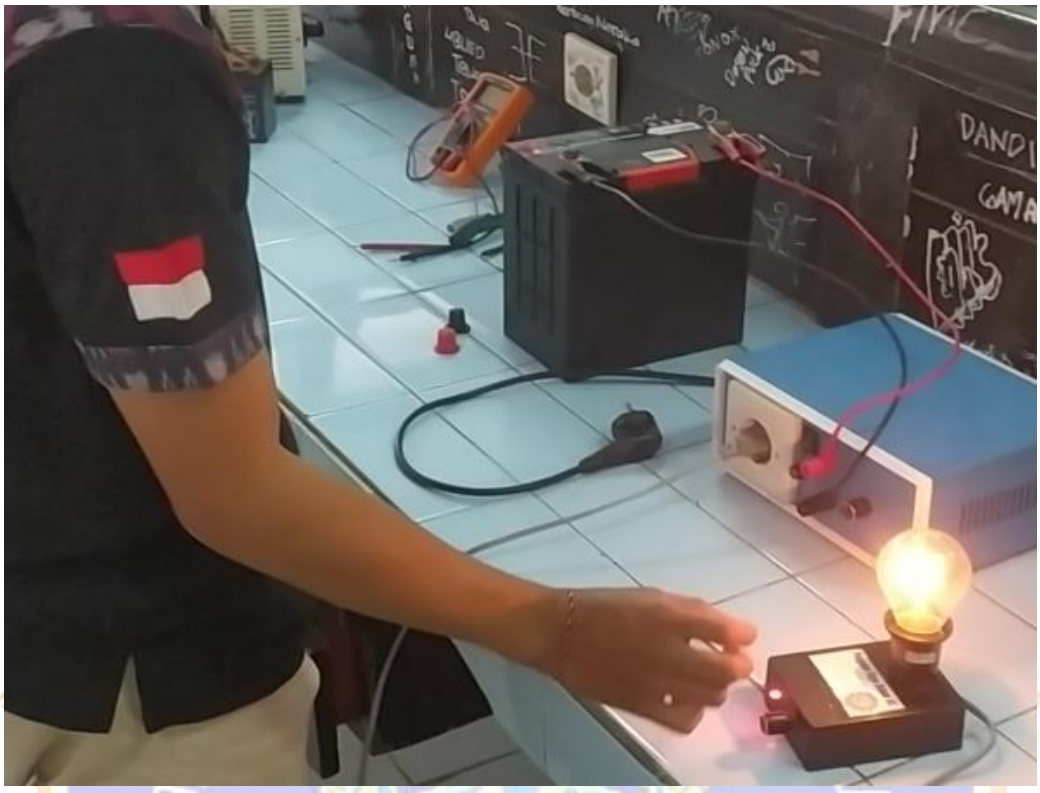
6. Dokumentasi pengujian rangkaian keseluruhan

7. Dokumentasi pengujian menggunakan bor tangan dengan daya 250 Watt



8. Dokumentasi pengujian menggunakan motor gerinda dengan daya 670 Watt

9. Dokumentasi pengujian menggunakan rangkaian dimmer



10. Dokumentasi hasil rangkaian inverter setelah dimasukan dalam kemasan

RIWAYAT HIDUP

I Nyoman Agus Darmawan lahir di Tabanan pada tanggal 08 Agustus 2002. Penulis lahir dari pasangan suami istri Bapak I Wayan Sukarta dan Ibu NI Nyoman Sueni. Penulis berkebangsaan Indonesia dan beragama Hindu. Kini penulis beralamat di Jalan Srikandi, Desa Bakti Seraga, Kecamatan Buleleng, Kabupaten Buleleng, Provinsi Bali. Penulis menyelesaikan pendidikan dasar di SD Negeri 2 Tengkudak dan lulus pada tahun 2015. Kemudian penulis melanjutkan di SMP Negeri 2 Penebel dan lulus pada tahun 2018. Pada tahun 2021, penulis lulus dari SMK Negeri 3 Tabanan jurusan Teknik Audio Video dan melanjutkan ke Diploma IV Jurusan Teknologi Industri Program Studi Teknologi Rekayasa Sistem Elektronika di Universitas Pendidikan Ganesha. Pada semester akhir tahun 2024 penulis telah menyelesaikan Tugas Akhir yang berjudul "Rancang Bangun Inverter Satu Phasa Untuk Sistem Penggerak Motor Listrik Tenaga Surya Pada Perahu Nelayan". Selanjutnya, mulai tahun 2024 sampai dengan penulisan skripsi ini, penulis masih terdaftar sebagai mahasiswa Program Diploma IV Teknologi Rekayasa Sistem Elektronika di Universitas Pendidikan Ganesha.