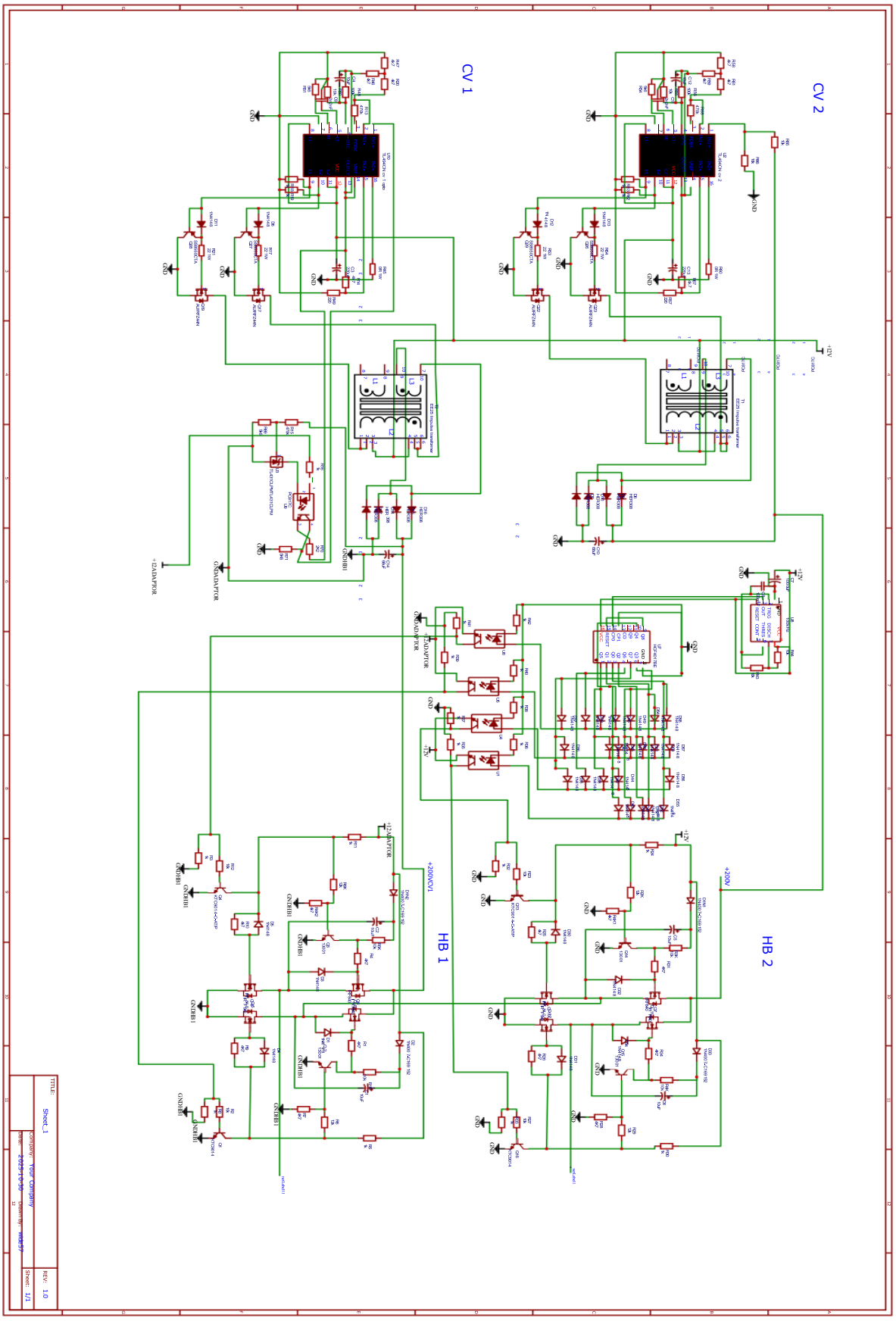
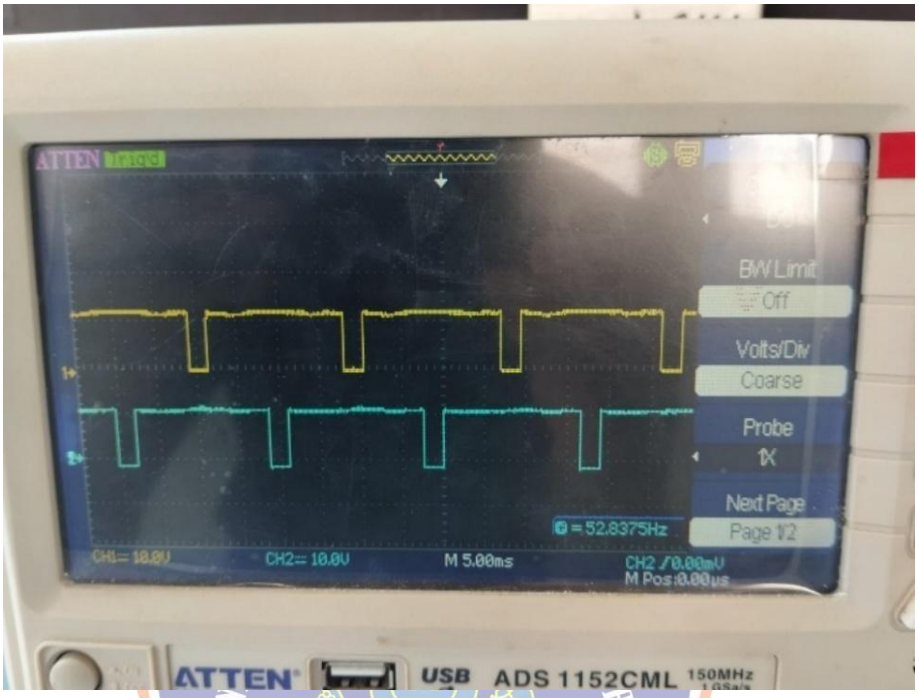
DAFTAR LAMPIRAN

Lampiran A Skematik Inverter 5 Tingkat

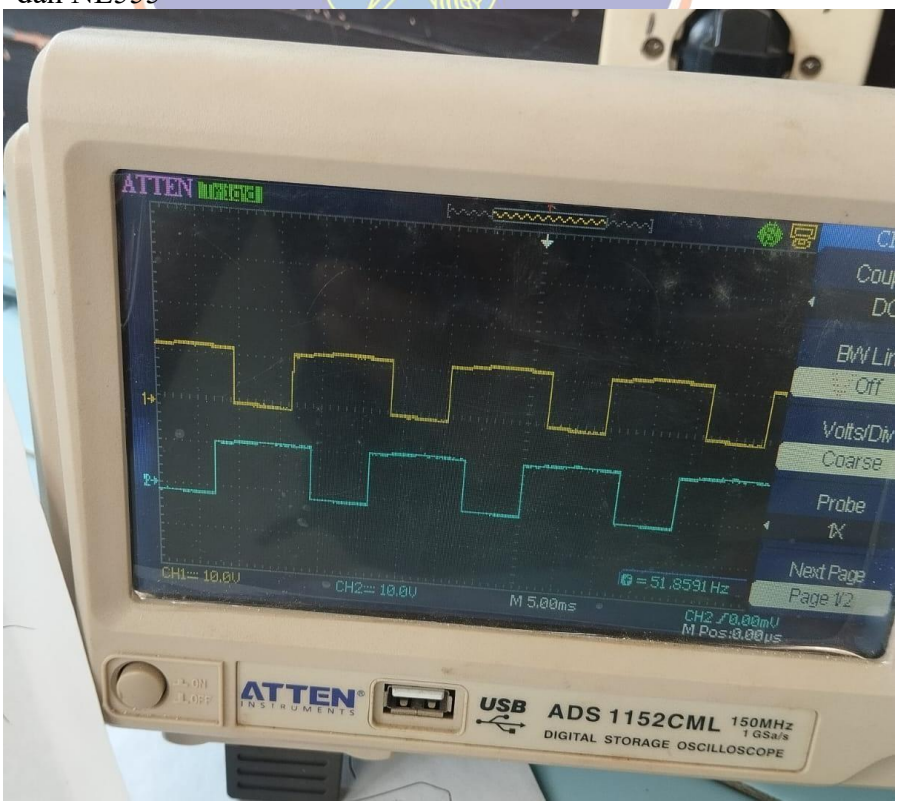


Lampiran B Pengujian Alat

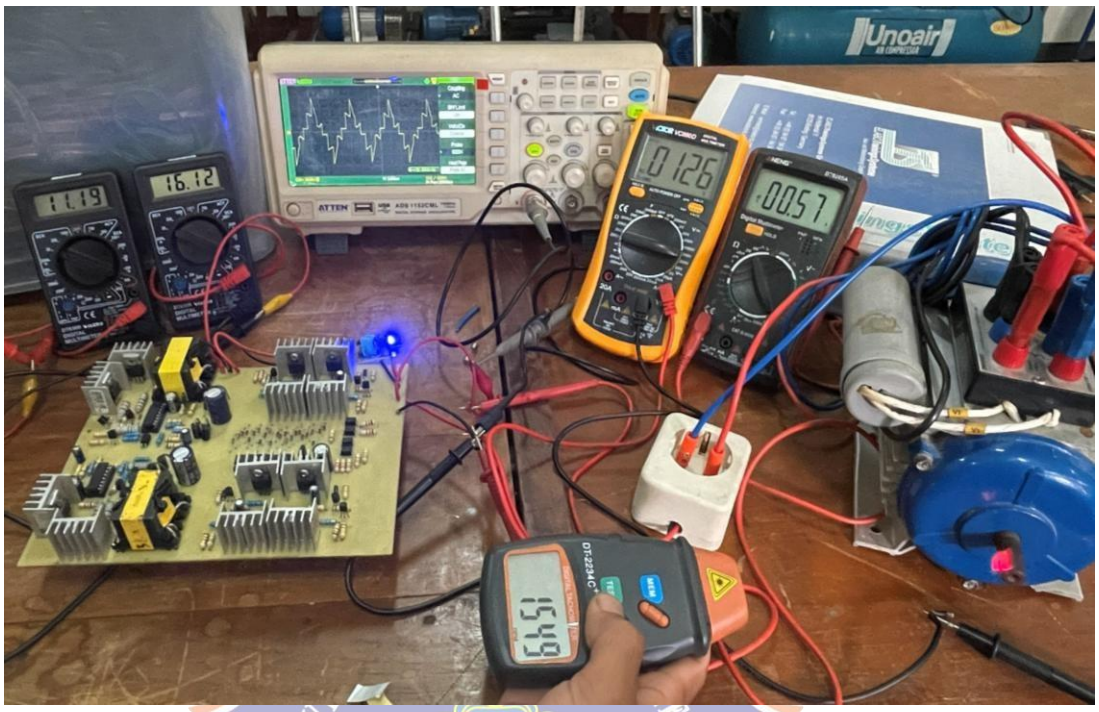
a. Dokumentasi Pengujian rancangan gelombang keluaran dengan IC 4017 dan NE555



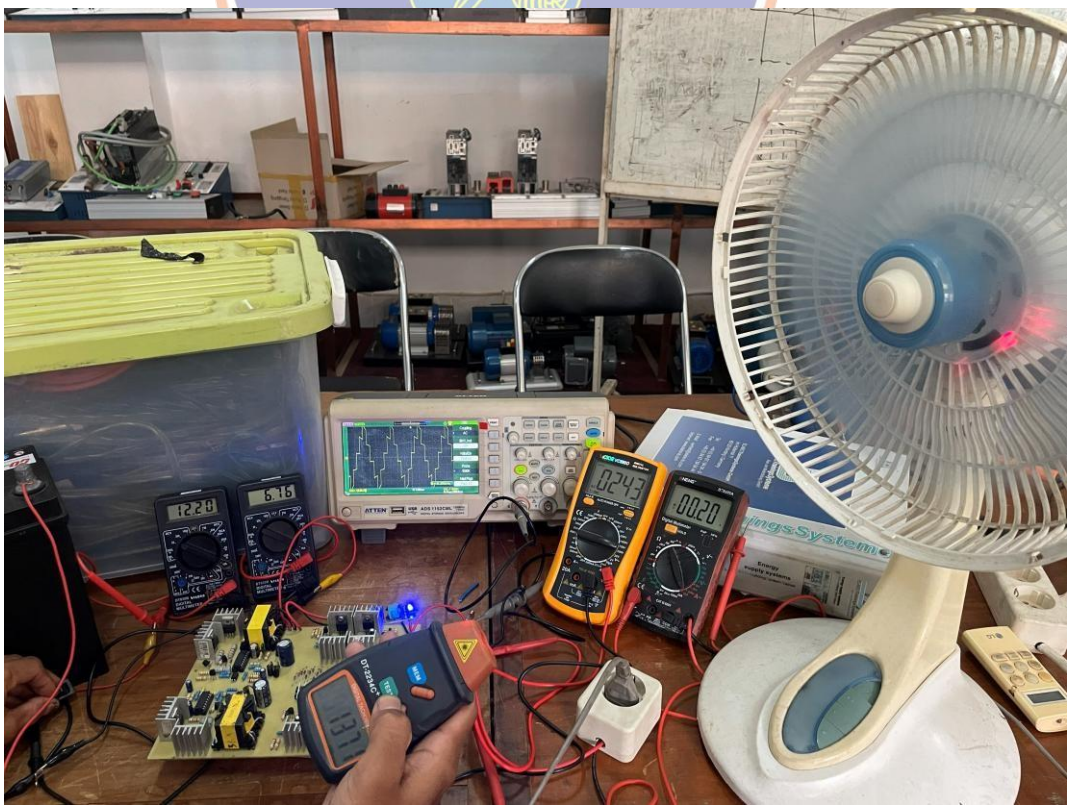
b. Dokumentasi Pengujian rancangan gelombang keluaran dengan IC 4017 dan NE555



c. Lampiran Foto Uji Coba Alat menggunakan beban induktif motor 1 phasa 120 W



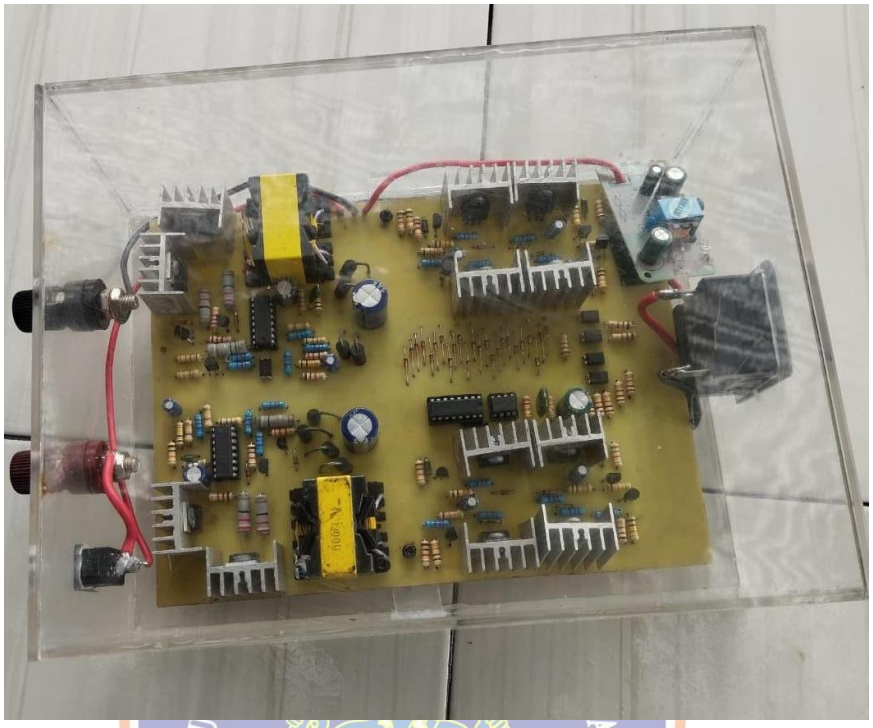
d. Lampiran Foto Uji Coba Alat menggunakan beban induktif Kipas Angin 45 W



e. Lampiran foto pengujian dengan beban resistif dari 40 W- 300 W

Lampiran C Hasil Akhir Alat

a. Foto dari atas



b. Foto dari samping

Lampiran D Data Sheet Komponen

a. Datasheet IC CD4017

FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

CD4017BC • CD4022BC
Decade Counter/Divider with 10 Decoded Outputs • Divide-by-8 Counter/Divider with 8 Decoded Outputs

General Description

The CD4017BC is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit.

The CD4022BC is a 4-stage divide-by-8 Johnson counter with 8 decoded outputs and a carry-out bit.

These counters are cleared to their zero count by a logical "1" on their reset line. These counters are advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the CD4017BC and CD4022BC permits medium speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10/8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power Fan out of 2 driving 74L
  TTL compatibility: or 1 driving 74LS
- Medium speed operation: 5.0 MHz (typ.)
  with 10V V_{DD}
- Low power: 10 µW (typ.)
- Fully static operation

Applications

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

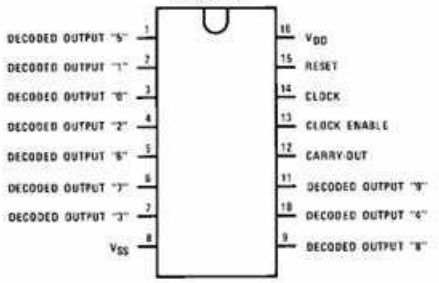
Ordering Code:

Order Number	Package Number	Package Description
CD4017BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4017BCSJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4017BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD4022BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4022BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

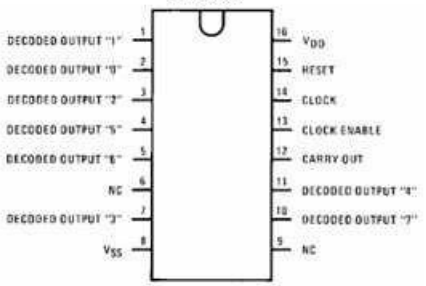
Connection Diagrams

Pin Assignments for DIP, SOIC and SOP
CD4017B



Top View

Pin Assignments for DIP and SOIC
CD4022B



Top View

 DS005950.prf www.fairchildsemi.com

Gambar D.1 Konfigurasi Pin IC CD4017BCN (PDIP 16 Pin)
Sumber: Fairchild Semiconductor, 1999

Absolute Maximum Ratings (Note 1)

(Note 2)

DC Supply Voltage (V_{DD})	−0.5 V_{DC} to +18 V_{DC}
Input Voltage (V_{IN})	−0.5 V_{DC} to V_{DD} +0.5 V_{DC}
Storage Temperature (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	+3 V_{DC} to +15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	−40°C to +85°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device	V_{DD} = 5V		20		0.5	20		150	µA
	Current	V_{DD} = 10V		40		1.0	40		300	µA
		V_{DD} = 15V		80		5.0	80		600	µA
V_{OL}	LOW Level	$\|I_O\|$ < 1.0 µA								
	Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level	$\|I_O\|$ < 1.0 µA								
	Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	LOW Level	$\|I_O\|$ < 1.0 µA								
	Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	HIGH Level	$\|I_O\|$ < 1.0 µA								
	Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	LOW Level Output	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
	Current (Note 3)	V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	HIGH Level Output	V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16	−0.36		−0.12		mA
	Current (Note 3)	V_{DD} = 10V, V_O = 9.5V	−0.5		−0.4	−0.9		−0.3		mA
		V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2	−3.5		−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	µA

Note 3: I_{OL} and I_{OH} are tested one output at a time.

Gambar D.2 Karakteristik Listrik DC IC CD4017
Sumber: Fairchild Semiconductor, 1999

AC Electrical Characteristics (Note 4)

T_A = 25°C, C_L = 50 pF, R_L = 200k, t_{rCL} and t_{fCL} = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CLOCK OPERATION							
t_{PHL}, t_{PLH}	Propagation Delay Time Carry Out Line	V_{DD} = 5V			415	800	ns
		V_{DD} = 10V			160	320	ns
		V_{DD} = 15V			130	250	ns
	Carry Out Line	V_{DD} = 5V			240	480	ns
		V_{DD} = 10V	C_L = 15 pF		85	170	ns
		V_{DD} = 15V			70	140	ns
	Decode Out Lines	V_{DD} = 5V			500	1000	ns
		V_{DD} = 10V			200	400	ns
		V_{DD} = 15V			160	320	ns
t_{TLH}, t_{THL}	Transition Time Carry Out and Decode Out Lines						
	t_{TLH}	V_{DD} = 5V			200	360	ns
		V_{DD} = 10V			100	180	ns
		V_{DD} = 15V			80	130	ns
	t_{THL}	V_{DD} = 5V			100	200	ns
		V_{DD} = 10V			50	100	ns
		V_{DD} = 15V			40	80	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	Measured with	1.0	2		MHz
		V_{DD} = 10V	Respect to Carry	2.5	5		MHz
		V_{DD} = 15V	Output Line	3.0	6		MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V			125	250	ns
		V_{DD} = 10V			45	90	ns
		V_{DD} = 15V			35	70	ns
t_{rCL}, t_{fCL}	Clock Rise and Fall Time	V_{DD} = 5V				20	µs
		V_{DD} = 10V				15	µs
		V_{DD} = 15V				5	µs
t_{SU}	Minimum Clock Inhibit Data Setup Time	V_{DD} = 5V			120	240	ns
		V_{DD} = 10V			40	80	ns
		V_{DD} = 15V			32	65	ns
C_{IN}	Average Input Capacitance				5	7.5	pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

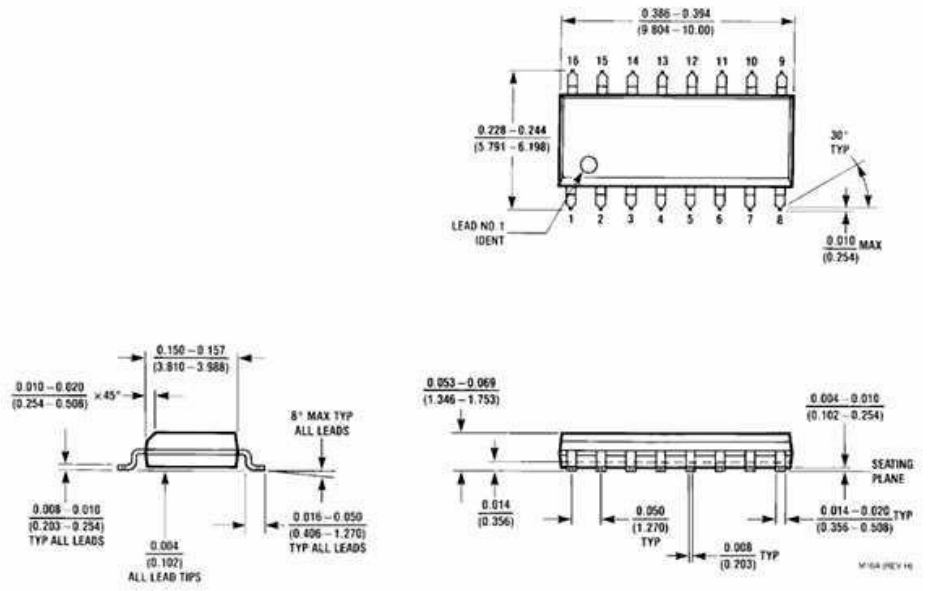
AC Electrical Characteristics (Note 4)

T_A = 25°C, C_L = 50 pF, R_L = 200k, t_{rCL} and t_{fCL} = 20 ns, unless otherwise specified

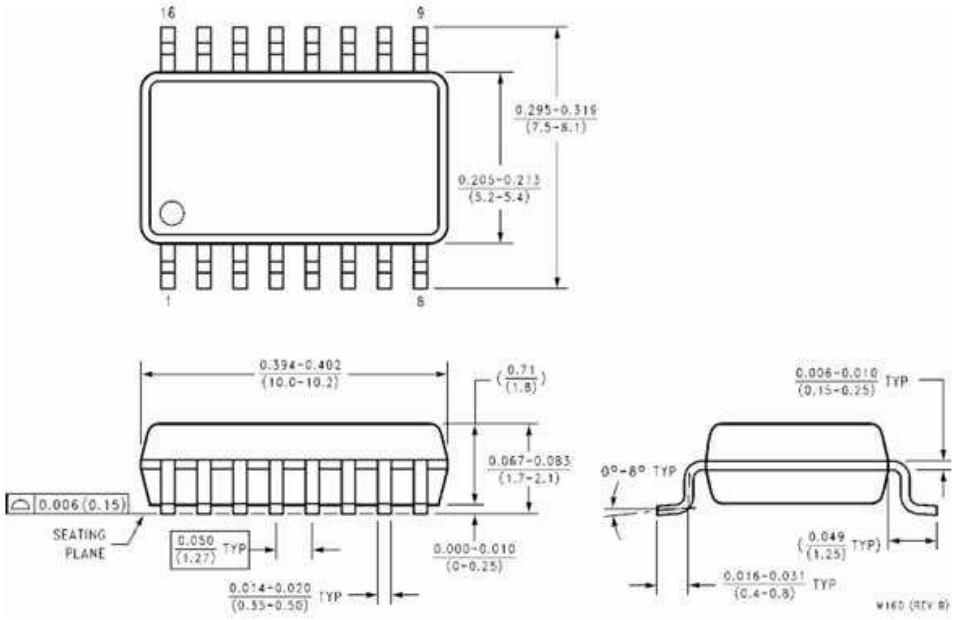
Symbol	Parameter	Conditions		Min	Typ	Max	Units
RESET OPERATION							
t_{PHL}, t_{PLH}	Propagation Delay Time						
	Carry Out Line	V_{DD} = 5V			415	800	ns
		V_{DD} = 10V			160	320	ns
		V_{DD} = 15V			130	250	ns
	Carry Out Line	V_{DD} = 5V			240	480	ns
		V_{DD} = 10V	C_L = 15 pF		85	170	ns
		V_{DD} = 15V			70	140	ns
	Decode Out Lines	V_{DD} = 5V			500	1000	ns
		V_{DD} = 10V			200	400	ns
		V_{DD} = 15V			160	320	ns
t_W	Minimum Reset	V_{DD} = 5V			200	400	ns
	Pulse Width	V_{DD} = 10V			70	140	ns
		V_{DD} = 15V			55	110	ns
t_{REM}	Minimum Reset	V_{DD} = 5V			75	150	ns
	Removal Time	V_{DD} = 10V			30	60	ns
		V_{DD} = 15V			25	50	ns

Gambar D.3 Karakteristik Listrik AC IC CD4017
Sumber: Fairchild Semiconductor, 1999

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A



16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

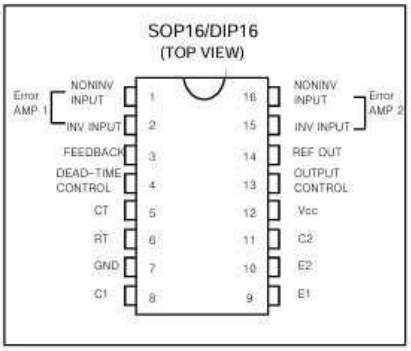
Gambar D.4 Dimensi dan Kemasan IC CD4017BCN (PDIP 16 Pin)
Sumber: Fairchild Semiconductor, 1999

b. Datasheet IC TL494

Pulse-Width-Modulation Control Circuits TL494

FEATURES

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for 200 Ma Sink or Source Current
- Output Control Selects Single-Ended or Push-Pull Operation
- Internal Circuitry Prohibits Double Pulse at Either Output
- Variable Dead-Time Provides Control over Total Range
- Internal Regulator Provides a Stable 5-V Reference Supply,5%
- Circuit Architecture Allows Easy Synchronization



DESCRIPTION

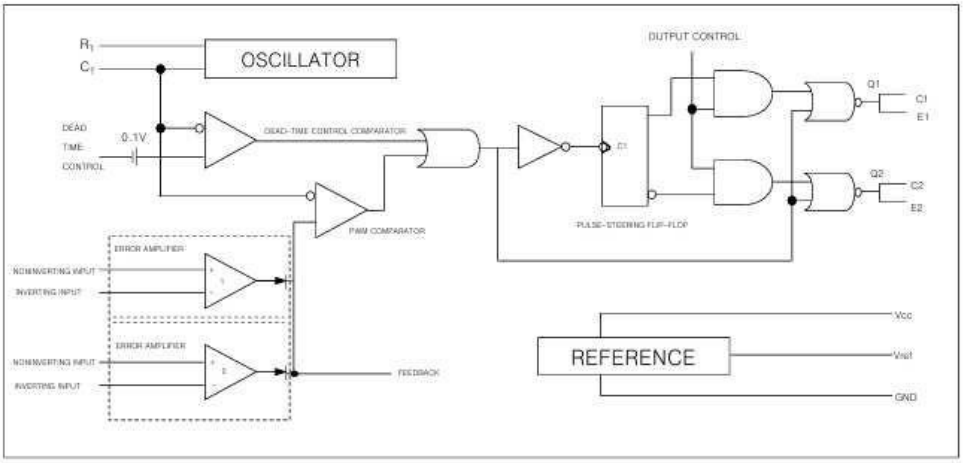
The TL494 incorporate on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control, these devices offer the systems engineer the flexibility to tailor the power supply control circuitry to his application.
The TL494 contains an error amplifier, an on-chip adjustable oscillator, a dead-time control comparator, pulse-steering control flip-flop, a 5-volt, 5% precision regulator, and output-control circuit.

ORDERING INFORMATION

Device	Package
TL494D	16 SOP
TL494N	18 DIP

The error amplifier exhibits a common-mode voltage range from -0.3 volts to Vcc -2 volts. The dead-time control comparator has a fixed offset that provides approximately 5% dead time when externally altered. The on-chip oscillator may be bypassed by terminating R_T (pin 6) to the reference output and providing a sawtooth in put to CT (pin 5), or it may be used to drive the common circuits in synchronous multiple-rail power supplies. The uncommited output transistors provide either common-emitter or emitter-follower output capability. Each Device provides for push-pull or single-ended output operation, which may be selected through the output-control funct -ion. The architecture of these devices prohibits the possibility of either output being pulsed twice during push -pull operation.

Functional Block Diagram



Mar. 2006-Rev08 HTC

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Gambar D.5 Konfigurasi Pin dan Diagram Blok IC TL494

Sumber : HTC, 2006

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE

Rating	Value	Unit
Supply voltage, Vcc	41	V
Amplifier input voltage	Vcc +0.3	
Collector output voltage	41	
Collector output current	250	mA
Operating free-air temperature range	0 to 70	°C
Storage temperature range	-65 to 150	
Lead temperature 1,6 mm from case for 10 seconds	260	

RECOMMENDED OPERATING CONDITIONS

Parameter	Value		Unit
	MIN	MAX	
Supply voltage, Vcc	7	40	V
Amplifier input voltage, Vi	-0.3	Vcc -2	
Collector output voltage, Vo		40	
Collector output current (each transistor)		200	mA
Current into feedback terminal		0.3	
Timing capacitor, C_T	0.47	10000	nF
Timing resistor, R_T	1.8	500	KΩ
Oscillator frequency	1	300	KHz
Operating free-air temperature, T_A	0	70	°C

Electrical characteristics over recommended operatng free-air temperature range,
Vcc=15V, f= 10 kHz(unless otherwise noted).

Parameter	Test Conditions*	Value			Unit
		MIN	TYP**	MAX	
Output voltage (Vref)	Io = 1mA	4.75	5	5.25	V
Input regulation	Vcc = 7V to 40 V		2	25	mV
Output regulation	Io = 1mA to 10mA		1	15	
Output voltage change with temperature	T_A = MIN to MAX		0.2	1	%
Short-circuit output current***	Vref = 0		35		mA

Oscillator section (See Figure 1)

Parameter	Test Conditions*	Value			Unit
		MIN	TYP**	MAX	
Frequency	C_T=0.01μF, R_T=12KΩ		10		KHz
Standard deviation of frequency****	All values of Vcc, C_T, R_T, and T_A constant		10		%
Frequency change with voltage	Vcc=7V to 40V, T_A=25oC		0.1		
Frequency change with temperature****	C_T=0.01μF, R_T=12KΩ, T_A = MIN to MAX			1	

Gambar D.6 Karakteristik Batas Operasi IC TL494

Sumber : HTC, 2006

Pulse-Width-Modulation Control Circuits TL494

Electrical characteristics over recommended operating free-air temperature range, Vcc=15V, f=10kHz (unless otherwise noted)

Amplifier section (See Figure 2)

SYMBOL	TEST CONDITIONS	MIN.	TYP**	MAX.	UNIT
Input offset voltage	Vo(pin 3)=2.5V		2	10	mV
Input offset current	Vo(pin 3)=2.5V		25	250	nA
Input bias current	Vo(pin 3)=2.5V		0.2	1	μA
Common-mode input voltage range	Vcc = 7V to 40V	-0.3~-2			V
Open-loop voltage amplification	Vo=3V, R_L=2KΩ, Vo=0.5~3.5V	70	95		dB
Unity-gain bandwidth	Vo=0.5~3.5V, R_L=2KΩ		800		kHz
Common-mode rejection ratio	Vo= 40V, T_A= 25°C	65	80		dB
Output sink current (pin 3)	V_{ID}=-15mV~-5V, $V_{(pin3)}$=0.7V	0.3	0.7		mA
Output source current (pin 3)	V_{ID}=15mV~5V, $V_{(pin3)}$=3.5V	-2			mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

** All typical values except for parameter changes with temperature are at TA =25 oC

*** Duration of the short-circuit should not exceed one second.

**** Standard deviation is a measure of the statistical distribution about the mean as derived from the formula.

***** Temperature coefficient of timing capacitor and timing resistor not taken into account.

Output section

PARAMETER		TEST CONDITIONS	MIN.	TYP*	MAX.	UNIT
Collector off-state current		V_{CE}=40V, Vcc=40V		2	100	μA
Emitter off-state current		V_{CC}=V_C=40V, V_E=0			-100	
Collector-emitter saturation voltage	Common-emitter	V_E=0, I_C=200mA		1.1	1.3	V
	Emitter-follower	Vc=15V, I_E=-200mA		1.5	2.5	
Output control input current		V_I=Vref			3.5	mA

Dead-time control-section (See Figure 1)

PARAMETER	TEST CONDITIONS	MIN.	TYP*	MAX.	UNIT
Input bias current(pin4)	V_I=0 to 5.25V		-2	-10	μA
Maximum duty cycle, each output	$V_{I\ (pin\ 4)}$=0, C_T=0.1uF, R_T=12KΩ		45		%
Input threshold voltage(pin 4)	Zero duty cycle		3	3.3	V
	Maximum duty cycle	0			

PMW comparator section (See Figure 1)

PARAMETER	TEST CONDITIONS	MIN.	TYP*	MAX.	UNIT
Input threshold voltage (pin3)	Zero duty cycle		4	4.5	V
Input sink current (pin 3)	V(pin3) = 0.7V	0.3	0.7		mA

Total device

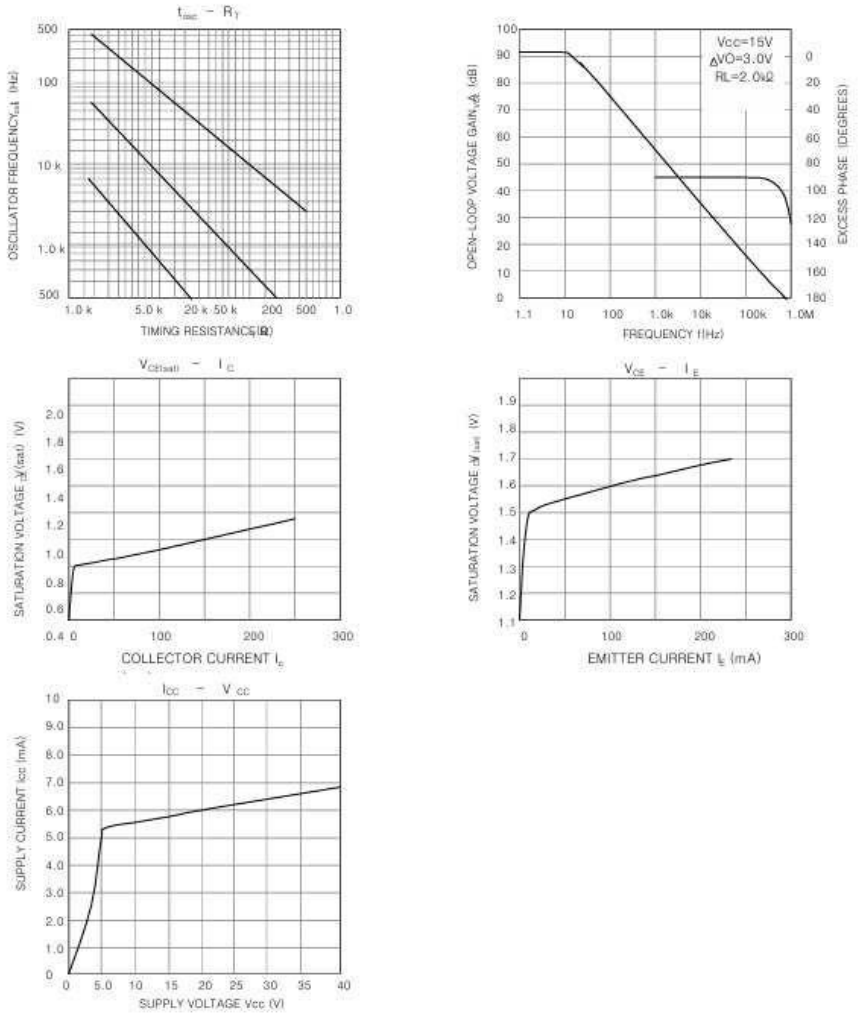
PARAMETER	TEST CONDITIONS		MIN.	TYP*	MAX.	UNIT
Standby supply current	Pin 6 at Vref, all other inputs and outputs open	V_{CC}=15V		6	10	mA
		V_{CC}=40V		9	15	
Average supply current	V_I(pin 4)= 2V			7.5		

Gambar D.7 Karakteristik Listrik IC TL494
Sumber : HTC, 2006

Switching characteristics, $T_A = 25°C$

PARAMETER	TEST CONDITIONS	MIN.	TYP*	MAX.	UNIT
Output voltage rise time	Common-emitter configuration		100	200	ns
Output voltage fall time			25	100	
Output voltage rise time	Emitter-follower configuration		100	200	
Output voltage fall time			40	100	

* All typical values except for temperature coefficient are at $T_A = 25°C$



Gambar D.8 Karakteristik Switching IC TL494
Sumber : HTC, 2006

c. Datasheet IRFZ44N

Suntac ELECTRONIC CORP

IRFZ44N

N-CHANNEL Power MOSFET

APPLICATION

- Buck Converter High Side Switch
- DC motor control , Ups ...etc , & other Application

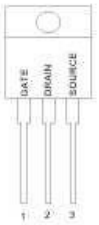
V_{DSS}	$R_{DS(ON)}$ Max.	I_D
55V	17.5mΩ	50A

FEATURES

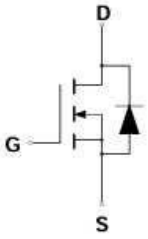
- Ultra Low ON Resistance
- Low Gate Charge
- Dynamic dv/dt Rating
- Inductive Switching Curves
- Peak Current vs Pulse Width Curve

PIN CONFIGURATION

TO-220
Front View



SYMBOL



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain to Source Voltage	V_{DSS}	55	V
Drain to Current – Continuous Tc = 25℃, V_{GS}@10V	I_D	50	A
– Continuous Tc = 100℃, V_{GS}@10V	I_D	35	
– Pulsed Tc = 25℃, V_{GS}@10V (Note 1)	I_{DM}	160	
Gate-to-Source Voltage – Continue	V_{GS}	±20	V
Total Power Dissipation	P_D	94	W
Derating Factor above 25℃		0.63	W/℃
Peak Diode Recovery dv/dt (Note 3)	dv/dt	5.0	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	℃
Repetitive Avalanche Energy (Note 1)	E_{AR}	9.4	mJ
Maximum Lead Temperature for Soldering Purposes	T_L	300	℃
Maximum Package Body for 10 seconds	T_{PKG}	260	℃
Avalanche Current (Note 1)	I_{AR}	25	A

THERMAL RESISTANCE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
$R_{\theta JC}$	Junction-to-case			1.5	℃/W	Water cooled heatsink, P_D adjusted for a peak junction temperature of +175℃
$R_{\theta JA}$	Junction-to-ambient			62	℃/W	1 cubic foot chamber, free air

Gambar D.9 Konfigurasi Pin dan Batas Maksimum MOSFET IRFZ44N
Sumber: Suntac Electronic Corp, t.t.

Suntac ELECTRONIC CORP

IRFZ44N

N-CHANNEL Power MOSFET

ORDERING INFORMATION

Part Number	Package
IRFZ44N	TO-220

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_J = 25℃.

Characteristic		Symbol	IRFZ44N Min	Typ	Max	Units
OFF Characteristics						
Drain-to-Source Breakdown Voltage (V_{GS} = 0 V, I_D = 250 μA)		V_{DSS}	55			V
Breakdown Voltage Temperature Coefficient (Reference to 25℃, I_D = 1mA)		$\Delta V_{DSS}/\Delta T_J$		0.058		V/℃
Drain-to-Source Leakage Current (V_{DS} = 55 V, V_{GS} = 0 V, T_J = 25℃)		I_{DSS}			25	μA
(V_{DS} = 44 V, V_{GS} = 0 V, T_J = 150℃)					250	
Gate-to-Source Forward Leakage (V_{GS} = 20 V)		I_{GSS}			100	nA
Gate-to-Source Reverse Leakage (V_{GS} = -20 V)		I_{GSS}			-100	nA
ON Characteristics						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	2.0		4.0	V
Static Drain-to-Source On-Resistance (Note 4) (V_{GS} = 10 V, I_D = 25A)		$R_{DS(on)}$			17.5	mΩ
Forward Transconductance (V_{DS} = 25 V, I_D = 25A) (Note 4)		g_{fs}	19			S
Dynamic Characteristics						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}		1470		pF
Output Capacitance		C_{oss}		360		pF
Reverse Transfer Capacitance		C_{rss}		88		pF
Total Gate Charge	(V_{DS} = 44 V, I_D = 25 A, V_{GS} = 10 V) (Note 2)	Q_g		63		nC
Gate-to-Source Charge		Q_{gs}		14		nC
Gate-to-Drain ("Miller") Charge		Q_{gd}		23		nC
Resistive Switching Characteristics						
Turn-On Delay Time	(V_{DD} = 28 V, I_D = 25 A, V_{GS} = 10 V, R_G = 12Ω) (Note 4)	$t_{d(on)}$		12		ns
Rise Time		t_{rise}		60		ns
Turn-Off Delay Time		$t_{d(off)}$		44		ns
Fall Time		t_{fall}		45		ns
Source-Drain Diode Characteristics						
Continuous Source Current (Body Diode)	Integral pn-diode in MOSFET (Note 1)	I_S			50	A
Pulse Source Current (Body Diode)		I_{SM}			160	A
Diode Forward On-Voltage	(I_S = 25A, V_{GS} = 0 V) (Note 4)	V_{SD}			1.3	V
Reverse Recovery Time	(I_F = 25A, V_{GS} = 0 V, d_i/d_t = 100A/μs) (Note 4)	t_{rr}		63	95	ns
Reverse Recovery Charge		Q_{rr}		170	260	nC

Notes:

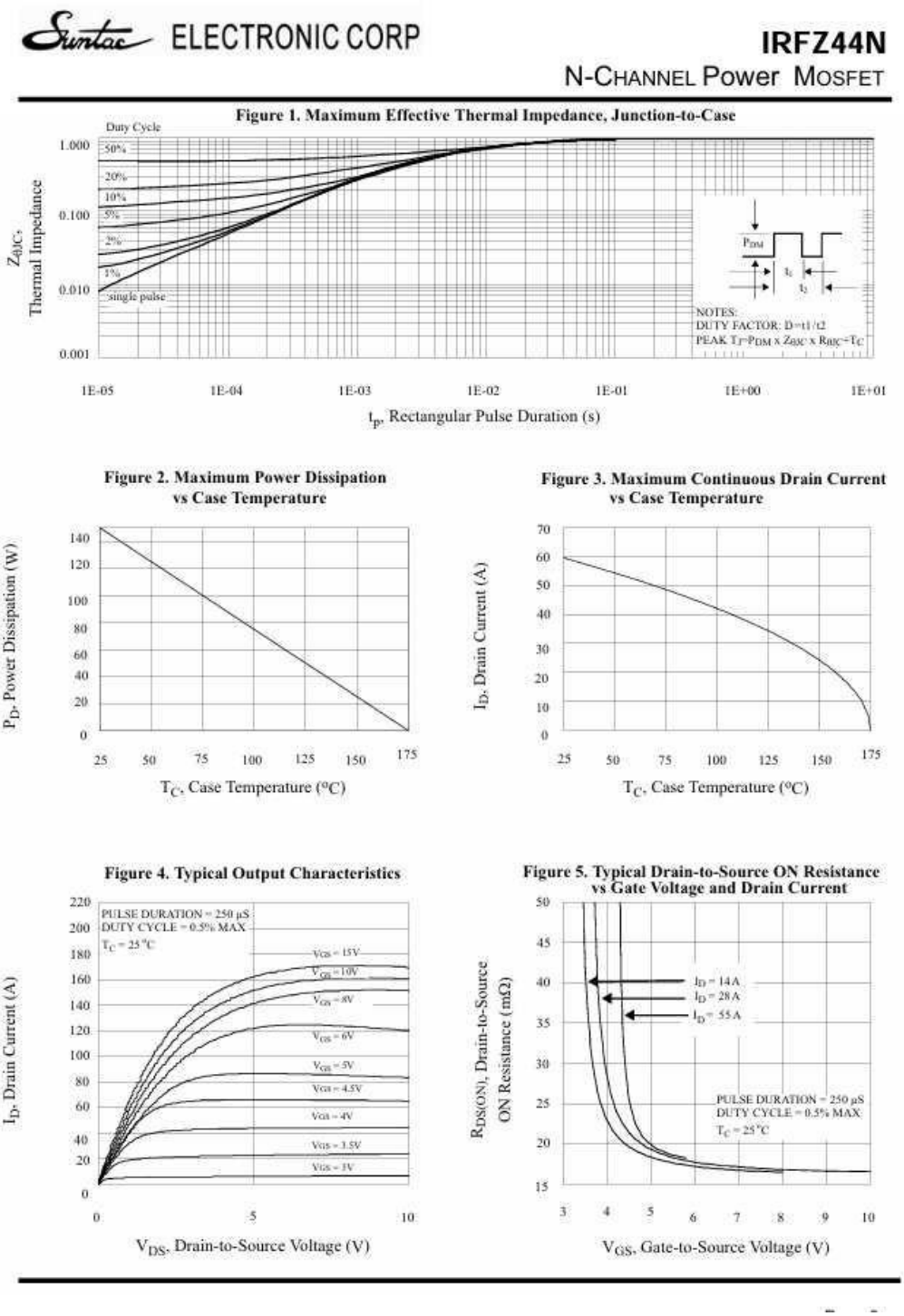
① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 1)

② Essentially independent of operating temerpature

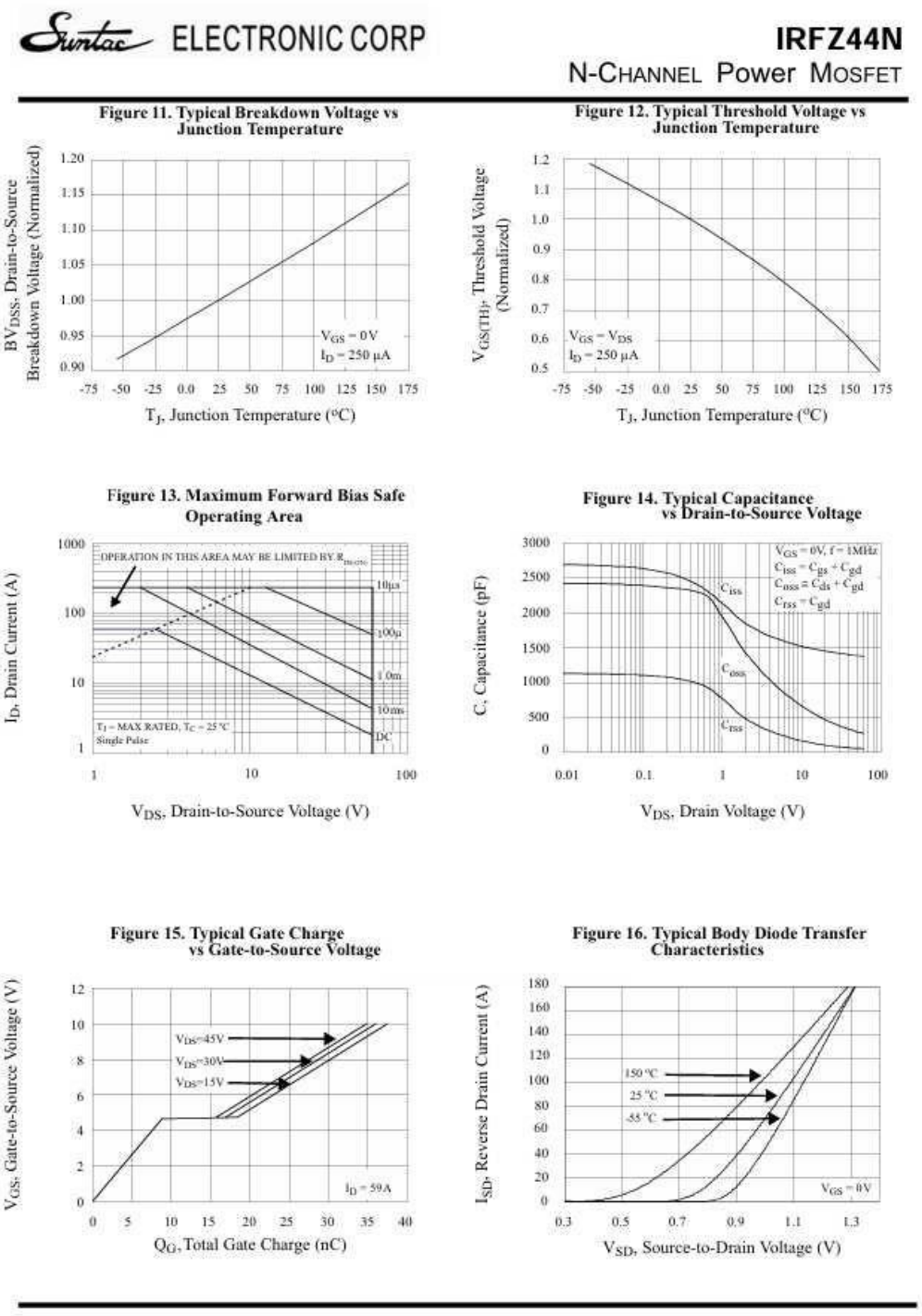
③ I_{SD} ≤ 25A, di/dt ≤ 230A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

Gambar D.10 Karakteristik Listrik MOSFET IRFZ44N
Sumber: Suntac Electronic Corp, t.t.



Gambar D.11 Karakteristik Termal dan Output MOSFET IRFZ44N
Sumber: Suntac Electronic Corp, t.t.



Gambar D.12 Karakteristik Switching dan Dioda MOSFET IRFZ44N
Sumber: Suntac Electronic Corp, t.t.

d. Datasheet IRFZ44N

NE555
SA555 - SE555

General-purpose single bipolar timers

Features

- Low turn-off time
- Maximum operating frequency greater than 500 kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- Output can source or sink up to 200 mA
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

Description

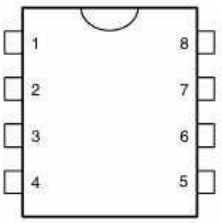
The NE555, SA555, and SE555 monolithic timing circuits are highly stable controllers capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor.

The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA.

N
DIP8
(Plastic package)

D
SO8
(Plastic micropackage)

Pin connections
(top view)



1 - GND
2 - Trigger
3 - Output
4 - Reset
5 - Control voltage
6 - Threshold
7 - Discharge
8 - V_{CC}

Gambar D.13 Konfigurasi Pin IC NE555
Sumber: STMicroelectronics, 2012

1 Schematic diagrams

Figure 1. Block diagram

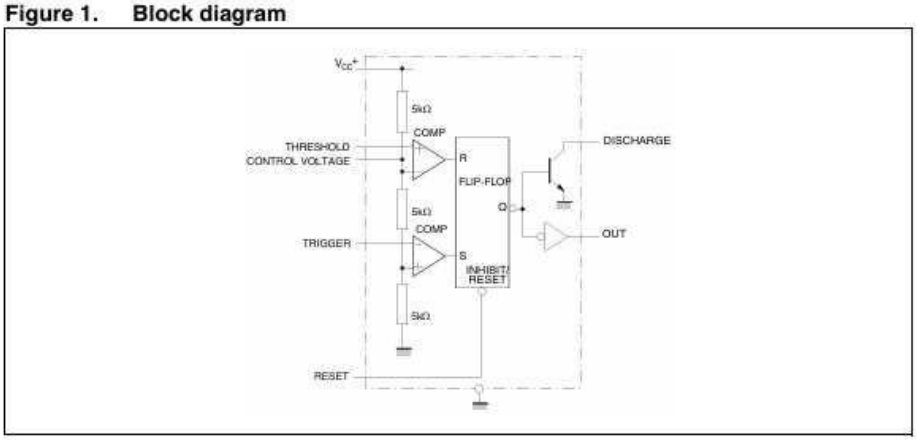
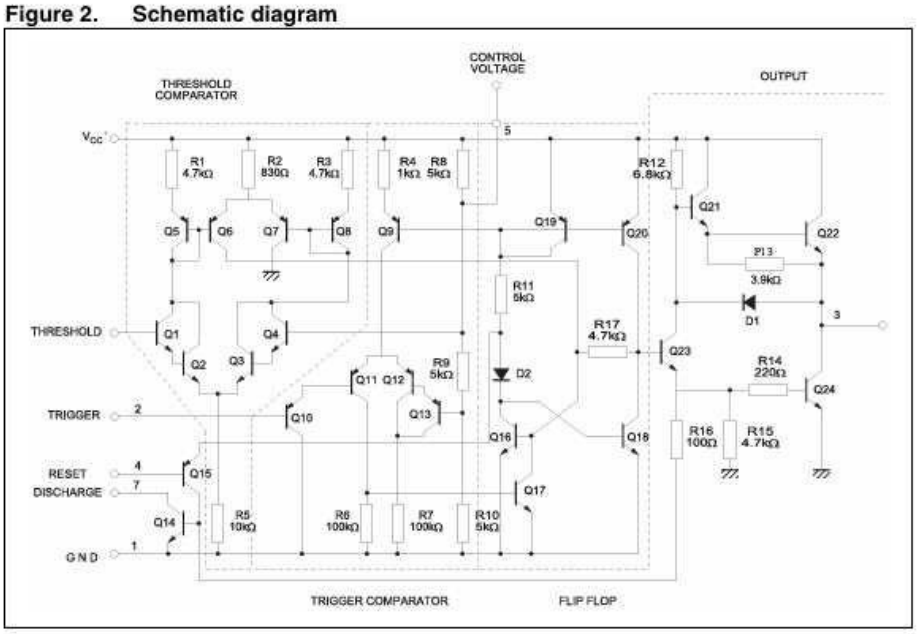


Figure 2. Schematic diagram



Gambar D.14 Diagram Blok dan Skematik Internal IC NE555
Sumber: STMicroelectronics, 2012

2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	18	V
I_{OUT}	Output current (sink & source)	±225	mA
R_{thja}	Thermal resistance junction to ambient(1) DIP8 SO-8	 85 125	°C/W
R_{thjc}	Thermal resistance junction to case(1) DIP8 SO-8	 41 40	°C/W
ESD	Human body model (HBM)(2)	1000	V
	Machine model (MM)(3)	100	
	Charged device model (CDM)(4)	1500	
	Latch-up immunity	200	mA
T_{LEAD}	Lead temperature (soldering 10 seconds)	260	°C
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature range	-65 to 150	°C

1. Short-circuits can cause excessive heating. These values are typical.
2. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
3. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
4. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage NE555 SA555 SE555	 4.5 to 16 4.5 to 16 4.5 to 18	V
V_{th}, V_{trig}, V_{cl}, V_{reset}	Maximum input voltage	V_{CC}	V
I_{OUT}	Output current (sink and source)	±200	mA
T_{oper}	Operating free air temperature range NE555 SA555 SE555	 0 to 70 -40 to 105 -55 to 125	°C

Gambar D.15 Batas Maksimum Operasi IC NE555
Sumber: STMicroelectronics, 2012

3 Electrical characteristics

Table 3. T_{amb} = +25° C, V_{CC} = +5 V to +15 V (unless otherwise specified)

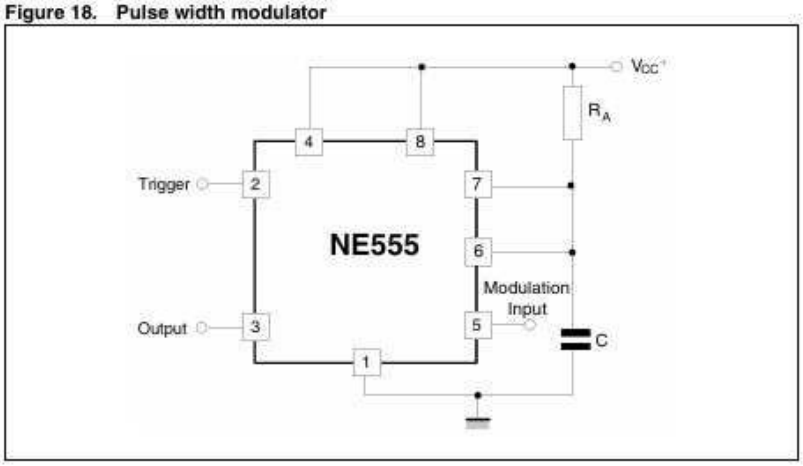
Symbol	Parameter	SE555			NE555 - SA555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CC}	Supply current ($R_L = \infty$) Low state V_{CC} = +5 V V_{CC} = +15 V High state V_{CC} = +5 V		3 10 2	5 12		3 10 2	6 15	mA
	Timing error (monostable) (R_A = 2 kΩ to 100 kΩ, C = 0.1 µF) Initial accuracy (1) Drift with temperature Drift with supply voltage		0.5 30 0.05	2 100 0.2		1 50 0.1	3 0.5	% ppm/°C %/V
	Timing error (astable) (R_A, R_B = 1 kΩ to 100 kΩ, C = 0.1 µF, V_{CC}= +15 V) Initial accuracy (1) Drift with temperature Drift with supply voltage		1.5 90 0.15			2.25 150 0.3		% ppm/°C %/V
V_{CL}	Control voltage level V_{CC} = +15 V V_{CC} = +5 V	9.6 2.9	10 3.33	10.4 3.8	9 2.6	10 3.33	11 4	V
V_{th}	Threshold voltage V_{CC} = +15 V V_{CC} = +5 V	9.4 2.7	10 3.33	10.6 4	8.8 2.4	10 3.33	11.2 4.2	V
I_{th}	Threshold current (2)		0.1	0.25		0.1	0.25	µA
V_{trig}	Trigger voltage V_{CC} = +15 V V_{CC} = +5 V	4.8 1.45	5 1.67	5.2 1.9	4.5 1.1	5 1.67	5.6 2.2	V
I_{trig}	Trigger current (V_{trig} = 0 V)		0.5	0.9		0.5	2.0	µA
V_{reset}	Reset voltage (3)	0.4	0.7	1	0.4	0.7	1	V
I_{reset}	Reset current V_{reset} = +0.4 V V_{reset} = 0 V		0.1 0.4	0.4 1		0.1 0.4	0.4 1.5	mA
V_{OL}	Low level output voltage V_{CC} = +15 V $I_{O(sink)}$ = 10 mA $I_{O(sink)}$ = 50 mA $I_{O(sink)}$ = 100 mA $I_{O(sink)}$ = 200 mA V_{CC} = +5 V $I_{O(sink)}$ = 8 mA $I_{O(sink)}$ = 5 mA		0.1 0.4 2 2.5 0.1 0.05	0.15 0.5 2.2 0.25 0.2		0.1 0.4 2 2.5 0.3 0.25	0.25 0.75 2.5 0.4 0.35	V

Gambar D.16 Karakteristik Listrik IC NE555
Sumber: STMicroelectronics, 2012

4.3 Pulse width modulator

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 18* shows the circuit.

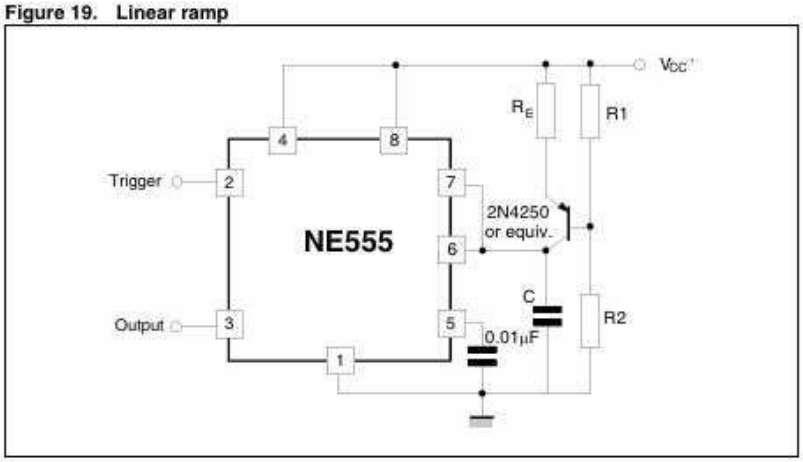
Figure 18. Pulse width modulator



4.4 Linear ramp

When the pull-up resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 19* shows a circuit configuration that will perform this function.

Figure 19. Linear ramp



Gambar D.17 Rangkaian PWM Menggunakan IC NE555
Sumber: STMicroelectronics, 2012

5.1 DIP8 package information

Figure 22. DIP8 package mechanical drawing

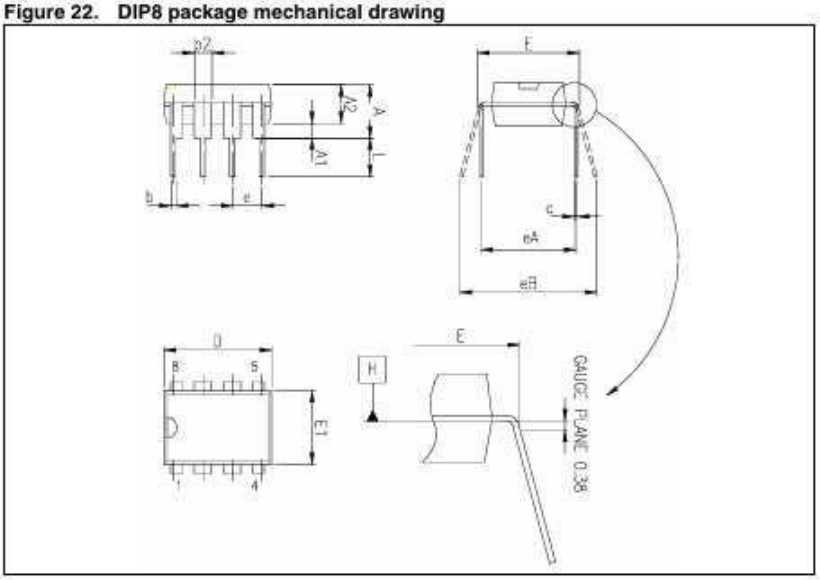
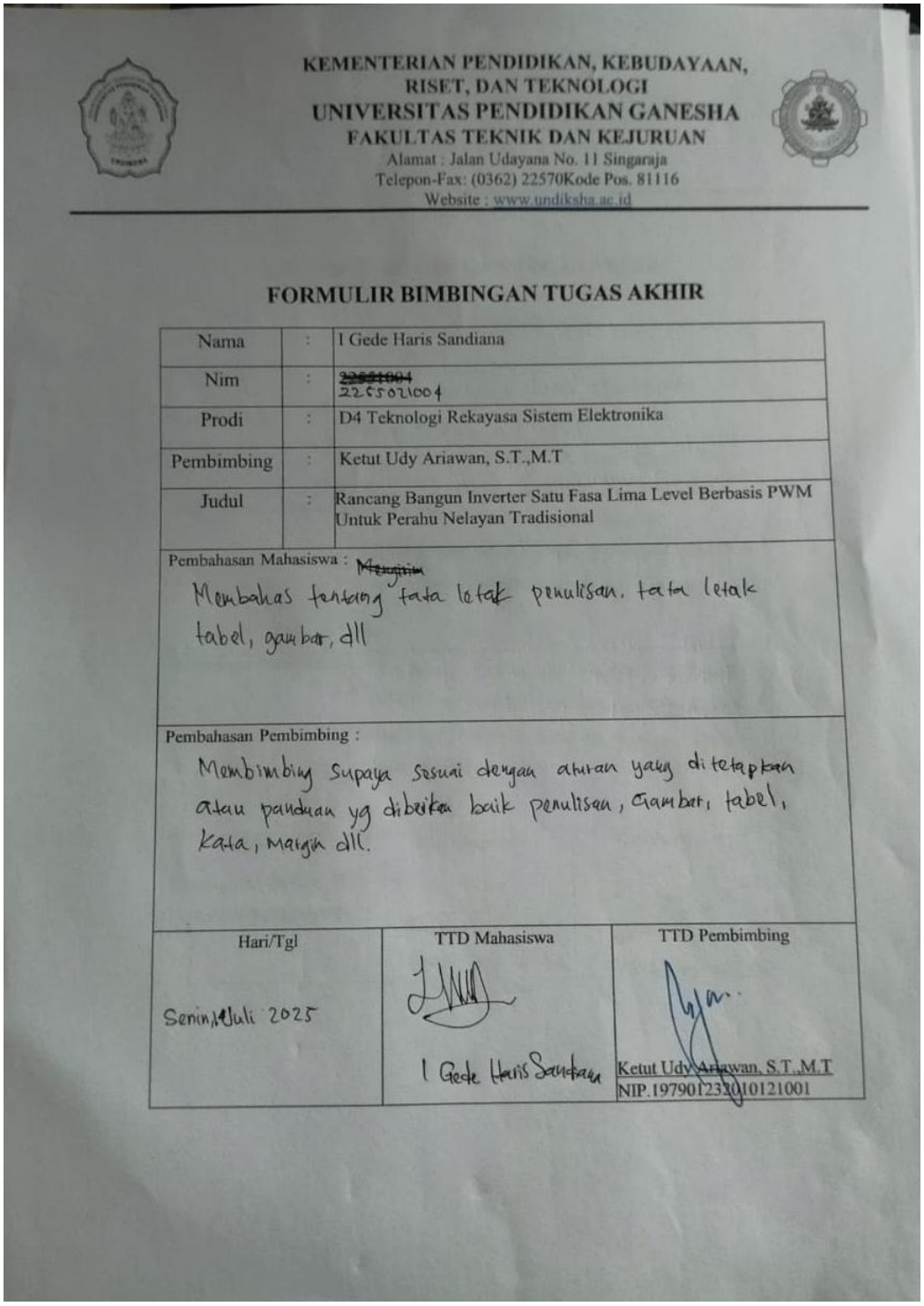


Table 4. DIP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
e		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150

Gambar D.18 Dimensi Kemasan DIP8 IC NE555
Sumber: STMicroelectronics, 2012

Lampiran E Formulir Bimbingan



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UNIVERSITAS PENDIDIKAN GANESHA
FAKULTAS TEKNIK DAN KEJURUAN
Alamat : Jalan Udayana No. 11 Singaraja
Telepon-Fax: (0362) 22570Kode Pos. 81116
Website : www.undiksha.ac.id

FORMULIR BIMBINGAN TUGAS AKHIR

Nama	:	I Gede Haris Sandiana
Nim	:	~~2255021004~~ 2255021004
Prodi	:	D4 Teknologi Rekayasa Sistem Elektronika
Pembimbing	:	Ketut Udy Ariawan, S.T.,M.T
Judul	:	Rancang Bangun Inverter Satu Fasa Lima Level Berbasis PWM Untuk Perahu Nelayan Tradisional

Pembahasan Mahasiswa : ~~Mengirim~~
Membahas tentang tata letak penulisan. tata letak tabel, gambar, dll

Pembahasan Pembimbing :
Membimbing supaya sesuai dengan aturan yang ditetapkan atau panduan yg diberikan baik penulisan, gambar, tabel, kata, margin dll.

Hari/Tgl	TTD Mahasiswa	TTD Pembimbing
Senin, 14 Juli 2025	I Gede Haris Sandiana	Ketut Udy Ariawan, S.T.,M.T NIP.197901232010121001

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RISET, DAN TEKNOLOGI
UNIVERSITAS PENDIDIKAN GANESHA
FAKULTAS TEKNIK DAN KEJURUAN
Alamat : Jalan Udayana No. 11 Singaraja
Telepon-Fax: (0362) 22570Kode Pos. 81116
Website : www.undiksha.ac.id

FORMULIR BIMBINGAN TUGAS AKHIR

Nama	:	I Gede Haris Sandiana
Nim	:	2255021004
Prodi	:	Teknologi Rekayasa Sistem Elektronika
Pembimbing	:	I Gede Nurhayata, S.T, M.T.
Judul	:	Rancang Bangun Inverter 1 fasa 5 level Berbasis PWM untuk Perahu Nelayan Tradisional

Pembahasan Mahasiswa :
- Melakukan Revisi Bab 2 dan 3
- Menambahkan tabel hasil pengujian inverter
- Menambahkan data dengan grafik

Pembahasan Pembimbing :
- Topologi terhadap inverter 5 level sudah dijelaskan di bab 2, lanjut bab 4
- Hasil uji sudah lengkap dengan tabel dan grafik

Hari/Tgl	TDD Mahasiswa	TDD Pembimbing
Senin, 29 Desember 2025 ~~Senin 29 [redacted] 2025~~	I Gede Haris Sandiana	I Gede Nurhayata, S.T., M.T.

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UNIVERSITAS PENDIDIKAN GANESHA
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Alamat : Jalan Udayana No. 11 Singaraja
Telepon-Fax: (0362) 22570Kode Pos. 81116
Website : www.undiksha.ac.id

FORMULIR BIMBINGAN TUGAS AKHIR

Nama	:	I Gede Haris Sandiana
Nim	:	~~2259108~~ 2255021004
Prodi	:	D4 Teknologi Rekayasa Sistem Elektronika
Pembimbing	:	Ketut Udy Ariawan, S.T.,M.T
Judul	:	Rancang Bangun Inverter Satu Fasa Lima Level Berbasis PWM Untuk Perahu Nelayan Tradisional

Pembahasan Mahasiswa :

- Pembuatan desain rancangan alat dan menentukan ukuran ~~supaya~~ box alat
- Penambahan referensi yang relevan

Pembahasan Pembimbing :

- Membahas rancangan dan desain alat supaya lebih ter struktur baik penempatan maupun ~~u~~ukuran dari box alat.
- Membahas pencarian referensi yang relevan dan sesuai

Hari/Tgl	TTD Mahasiswa	TTD Pembimbing
Senin, 5 Januari 2026	I Gede Haris Sandiana	Ketut Udy Ariawan, S.T.,M.T NIP.197901232010121001

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RISET, DAN TEKNOLOGI
UNIVERSITAS PENDIDIKAN GANESHA
FAKULTAS TEKNIK DAN KEJURUAN
Alamat : Jalan Udayana No. 11 Singaraja
Telepon-Fax: (0362) 22570Kode Pos. 81116
Website : www.undiksha.ac.id

FORMULIR BIMBINGAN TUGAS AKHIR

Nama	:	I Gede Haris Sandiana
Nim	:	2255021004
Prodi	:	Teknologi Rekayasa Sistem Elektronika
Pembimbing	:	I Gede Nurhayata, S.T.,M.T.
Judul	:	Rancang Bangun Inverter Satu Fasa Lima level Berbasis PWM untuk Perahu Nelayan Tradisional

Pembahasan Mahasiswa : ~~Pembuatan penentuan~~
Membahas Penempatan Rancangan Alat, Box Alat ~~output~~ dan penempatan per blok komponen

Pembahasan Pembimbing :
Membahas penempatan/Rancangan Alat supaya alat lebih praktis dan rapi. Dan jika dijadikan Media pembelajaran mudah dipahami untuk mahasiswa lain.

Hari/Tgl	TDD Mahasiswa	TDD Pembimbing
Senin, 5 Januari 2026	I Gede Haris Sandiana	I Gede Nurhayata S.T.,M.T.

RIWAYAT HIDUP

I Gede Haris Sandiana, lahir di Panji Anom, 13 April 2004. Penulis lahir dari pasangan suami istri Bapak Ketut Joniarka dan Ibu Ni Ketut Sujani. Penulis berkebangsaan Indonesia dan beragama Hindu. Kini penulis beralamat di Jalan Banjar Dinas Abasan RT 02 Desa Panji Anom, Kecamatan Buleleng, Kabupaten Buleleng, Provinsi Bali.

Penulis menyelesaikan pendidikan di SD Negeri 1 Panji Anom, dan lulus pada tahun 2016. Kemudian penulis melanjutkan di SMP Negeri 4 Singaraja, dan lulus pada tahun 2019. Pada tahun 2022, penulis lulus dari SMK N 3 Singaraja jurusan Teknik Mesin dan melanjutkan ke Diploma IV Program Studi Teknologi Rekayasa Sistem Elektronika di Universitas Pendidikan Ganesha. Penulis sampai saat ini masih mengerjakan Tugas Akhir yang berjudul “Rancang Bangun Inverter Satu Fasa Lima Level Berbasis PWM untuk Perahu Nelayan Tradisional”.

PERNYATAAN KEASLIAN TULISAN

Dengan ini saya menyatakan bahwa karya tulis yang berjudul "Rancang Bangun Inverter Satu Fasa Lima Level Berbasis PWM untuk Perahu Nelayan Tradisional" beserta seluruh isinya adalah benar-benar karya sendiri dan saya tidak melakukan penjiplakan dan pengutipan dengan cara-cara yang tidak sesuai dengan etika yang berlaku dalam masyarakat keilmuan. Atas pernyataan ini, saya siap menanggung risiko/sanksi yang dijatuhkan kepada saya apabila kemudian ditemukan adanya pelanggaran atas etika keilmuan dalam karya saya ini atau ada klaim terhadap keaslian karya saya ini.

Singaraja,

Yang membuat pernyataan,

I Gede Haris Sandiana

NIM. 2255021004